Name: Dr. Soumen Mallick

Department: Information Technology

Contact Nos.: 9800199933 / 9476148388

Qualifications: B.Tech, M.Tech, Ph.D

Designation: Assistant Professor (Grade II)

VIDWAN ID: 187682

Experience (Teaching / Research / Industry, in years): 15 years (Teaching)

Date of Joining at the Present Institution: 11/08/2010

Examinations Cleared: GATE in 2004

Qualifications Summary (Reverse chronological order):

Degree	Institute	From – To	Subjects
Ph.D	National Institute of Technology Durgapur	2014–2019	Optimal Sizing and Design of Analog CMOS Circuits using Evolutionary Optimization Techniques
M.Tech	Jadavpur University	2004–2007	VLSI Design & Microelectronics Technology
B.Tech	HIT, Haldia	2000–2004	Instrumentation Engineering
H.S	Simlapal Madan Mohan High School	1997–2000	Science
Secondary	Pukhuria High School	1992–1997	As per W.B.B.S.E Syllabus

Experience Summary (In chronological order):

Lecturer, BITM, Santiniketan, 20/07/2007-10/08/2010

Assistant Professor (Grade II), BCREC, Durgapur, 11/08/2010- Till Date

Specialization/Research Interest: Analog VLSI Design, Digital VLSI Design, Evolutionary Optimization Techniques.

Awards & Recognitions
Best paper/ scholarship/Position in university exam / awards while at industry/ other organizations etc.

N/A

Courses taught:

Theory: Basic Electronics Engineering, Analog Integrated Circuit, Industrial Instrumentation, Microelectronics & VLSI Technology, Power Electronics

Practical: Basic Electronics Engineering Lab, Analog Integrated Circuit Lab, VLSI Lab, Power Electronics Lab.

Online Mode of Teaching: Google Meet

Publications:

Journal:

1. **S. Mallick**, R. Kar, S. P. Ghoshal and D. Mandal, "Optimal sizing and design of CMOS analogue amplifier circuits using craziness-based particle swarm optimization", International Journal of Numerical Modelling, 2016, Vol. 29, No. 5, pp. 943-966, 1099-1204.
2. **S. Mallick**, R. Kar, D. Mandal and S. P. Ghoshal "CMOS analogue amplifier circuits optimisation using hybrid backtracking search algorithm with differential evolution", Journal of Experimental & Theoretical Artificial Intelligence, 2016, Vol. 28, No. 4, pp. 719-749, 1362-3079.
3. **S. Mallick**, R. Kar, D. Mandal and S. P. Ghoshal, "Optimal sizing of CMOS analog circuits using gravitational search algorithm with particle swarm optimization", International Journal of Machine Learning. & Cybernetics, 2017, Vol. 8, No. 1, pp. 309-331, February, 1868-8071.
4. **S. Mallick**, R. Kar, S. P. Ghoshal and D. Mandal, "SEOA-based optimal design of analogue CMOS amplifier circuits", International Journal of Bio-Inspired Computation, 2017, Vol. 9, No. 4, pp. 211-225, 1758-0374.

Conference:

1. **S. Mallick**, K. Sudhakar, R. Kar, D. Mandal, S.P. Ghoshal, "CMOS analog amplifier circuit sizing using opposition based harmony search algorithm", International Conference on Communication and Signal Processing (ICCSP), IEEE, April 6-8, 2016, International Conference, IEEE, Electronic ISBN: 978-1-5090-0396-9, Print on Demand (PoD) ISBN: 978-1-4673-8549-7, DOI: 10.1109/ICCSP.2016.7754428.
2. **S. Mallick**, K. Suman, R. Kar, D. Mandal, S. P. Ghoshal, "Sizing of two-stage Op-amp using OHS Algorithm", 5th International Electrical Engineering Congress (iEECON), March 8-10, 2017, International Conference, IEEE, Electronic ISBN: 978-1-5090-4666-9, Print on Demand (PoD) ISBN: 978-1-5090-4667-6, DOI: 10.1109/IEECON.2017.8075891.
3. **S. Mallick**, J. R. Akhil, A. Dasgupta, R. Kar, D. Mandal, S. P. Ghoshal, "Optimal design of 5.5 GHz CMOS LNA using hybrid fitness based adaptive DE with PSO", 5th International Electrical Engineering Congress (iEECON), March 8-10, 2017, International Conference, IEEE, Electronic ISBN: 978-1-5090-4666-9, Print on Demand (PoD) ISBN: 978-1-5090-4667- 6, DOI: 10.1109/IEECON.2017.8075890.

Book Chapter:

1. **S. Mallick**, R. Kar, D. Mandal, T. Dasgupta, S.P. Ghoshal, "Optimal Design of 2.4 GHz CMOS LNA Using PSO with Aging Leader and Challenger", pp. 291-303, Advances in Computer Communication and Computational Sciences, Springer Singapore, 2019, Print ISBN 978-981-13-0343-2, Online ISBN 978-981-13-0344-9

Supervision of Ph.D/M.Tech / B.Tech Projects:

B.Tech Projects:

Sl. No.	Name of students with University Roll No.	Name of the Supervisor	Title of the Project	Year
1	Saurabh Kumar (071200105035) Amit Kumar Singh (071200105015) Ankit Chakraborty (071200105023)	Dr. Soumen Mallick	Heartbeat measurement using piezoelectric accelerometer	2011
2	Moumita Basak (08120005011) Payel Chatterjee (08120005033) Souvik Bhattacharya (08120005036)	Dr. Soumen Mallick	Evaluation of drinking water quality of various parts of Durgapur area using statistical analysis	2012
3	Vipul Kumar Bhaskar (09120005036) Kumar Satyam (09120005041) Saurabh Sameer Sinha (09120005045)	Dr. Soumen Mallick	Digital temperature sensor	2013
4	Prateek Srivastava (12000510022) Shashi Kumar (12000510056)	Dr. Soumen Mallick	Microcontroller based digital clock	2014
5	Ahshan Ahmed Kausher (12000511006) Basher Jamil (12000511013) Shivam Kumar Gupta (12000511051) Swapnil Suman (12000511058)	Dr. Soumen Mallick	Smart classroom using Thermistor	2015
6	Arnab Das (12000512009) Debasish Dey (120005512014)	Dr. Soumen Mallick	Android based home automation system using bluetooth module HC-05	2016
7	Aditya Shekhar (12000513004) Arvind Kumar (12000513011) Kumar Aditya (12000513020)	Dr. Soumen Mallick	Street light intensity control using Aurdino UNO	2017
8	Juin Chakraborty (12005514006)	Dr. Soumen Mallick	Coin-based water controlling system	2018
9	Jaiprakash Kumar (12005515012) Shubham Mishra (12005515028)	Dr. Soumen Mallick	Controlling of Home Lights using Smartphone	2019
10	Swarnojyoti Banerjee (12005516003) Soumya Kanti Sarkar (12005516007) Sk. Asifuddin (12005516008) Ayan Ghosh (12005516029) Akash Das (12005516037)	Dr. Soumen Mallick	Automotive Irrigation System	2020

Invited Lectures: N/A

Participation in seminar/conference/symposium/workshop/discussion meeting

1. Participated Two-week ISTE Workshop on "Signal and Systems", From 2nd -12th January, 2014, Organized jointly by IIT Kharagpur and NIT Durgapur under the NMEICT.

2. Participated in the MHRD sponsored one-day workshop on NMEICT Awareness on 9th May, 2013.

Participation in faculty development programmes

1. Participated in the One-week FDP on "Behavioral Remodeling and use of ICT Tools for Classroom Delivery of Teachers", From 14th to 19th January, 2019, Organized by E & ICT Academy IIT Guwahati.

Organization of events (Dr. B. C. Roy Engineering College)

N/A

Participation in administrative committees (selected)

Working as a departmental co-ordinator of Training & Placement Cell since 2018.

Project Ideas Submitted to Govt. Agencies/ On-going Projects / Research Ideas under preparation & execution

N/A

Membership of professional bodies: IEEE, IETE, IEI, CSI, MGMI etc.

N/A