Name: Dr. ALOKE SAHA

Department:
Electronics & Communication Engineering

Contact Nos.: +91 8967627938

Qualifications: PhD

Designation: Assistant Professor

VIDWAN ID: 184948

Experience (Teaching/Research/Industry, in years):
Teaching: 15 years
Research: 14 years

Date of Joining at the Present Institution: 26/02/2009

Examinations Cleared: GATE -2004

Qualifications Summary (Reverse chronological order):

Degree	Board/ University/Institute	From	To	Subjects
PhD	BIT Mesra	2007	2015	VLSI Design
M.E.	BIT Mesra	2004	2006	Electronics & Communication Engineering
B. Tech	University of Kalyani	1999	2003	Electronics & Instrumentation Engineering
Higher Secondary	WB.C.H.S.E	1998	1999	Science (Physics, Chemistry, Mathematics, Biology)
Madhyamik	W.B.B.S.E	-	1997	Physical Science, Life Science, Mathematics, Bengali, English, History, Geography

Experience Summary (In chronological order):

Designation	*Institute/Organization*	*From*	*To*
Lecturer	BIT, Mesra, Ranchi	16.07.2006	25.02.2009
Assistant Professor	Dr. B. C. Roy Engineering College, Durgapur	26.02.2009	Present

Specialization/Research Interest:

Investigating speed-power efficient MVL (Multi Valued Logic) circuit as well as Double Base Number System (DBNS) for future digital computing application like IOT, ASIC solution for data security as well as medical electronics, Adaptive digital VLSI circuit for next generation smart Embedded Systems, Design for data security, Logic enhancement with latest technology like FinFET, CNTFET, Single Electron FET etc.

Awards & Recognitions
Best paper/ scholarship/Position in university exam / awards while at industry/ other organizations etc.

- Received scholarship of Rs. 60,000/- per year from AICTE for the period of two years (2004-2005) to complete Master of Engineering (M.E) from BIT Mesra.
- Innovative project award in Master of Engineering by Cadence Design Systems (I) Pvt. Ltd.(Cadence Design Contest 2005-2006)
- Entrepreneurship Week-India 2010 Championship Runner-up by National Entrepreneurship Network, India 2010.

Courses taught:

	BIT Mesra, Ranchi		**Dr. B. C. Roy Engineering College, Durgapur**	
	B.E.	M.E.	B. Tech	M. Tech
Theory	VLSI Design, Microelectronics Engineering, Semiconductor Devices, Pulse & Digital Circuits (PDC), Basic Electronics.	Embedded System	Digital System Design, CMOS VLSI Design, Analog Electronic Circuits, VLSI Circuit & Systems, EDA for VLSI Design, Embedded System, Basic Electronics, Microelectronics & VLSI Design, Digital Signal Processing, Analog Communication.	Digital IC Design, Processor Architecture for VLSI, Advanced VLSI Design, Mobile communication
Practical	VLSI Design Lab., Pulse & Digital Circuit Lab., Basic Electronics Lab., Circuit Simulation Lab., Digital Logic Lab.	-	Digital System Design Lab., Analog Electronic Circuits Lab., VLSI Circuit & Systems Lab., EDA Lab., Basic Electronics Lab., VLSI Design Lab.,	CAD Tools for VLSI Design Lab., Microelectronic Technology Lab.

Online Mode of Teaching:

- Theory and Laboratory classes are conducted using Google-meet.
- Study materials (Lecture notes & PPT) are sent through email.
- Class performance is observed through class assignments as well as post lecture assignments through Google form.
- Continuous Assessment (CA) for theory classes have been carried out in the form of Class Test/Assignment/Viva using Google-meet.
- Laboratory Examinations have been conducted using Google-meet.

Publications:

Journal:

1. **Aloke Saha**, Narendra Deo Singh and Dipankar Pal, "Efficient ternary comparator on CMOS technology," *Microelectronics Journal, Elsevier,* March **2021**, vol. 109, pp. 105005 (1-9), ISSN: 0026-2692. DOI: 10.1016/j.mejo.2021.105005. Impact Factor: **1.605**.

   http://mjl.clarivate.com/cgi-bin/jrnlst/jlresults.cgi?PC=MASTER&ISSN=*0026-2692

2. **Aloke Saha**, Rakesh Kumar Singh, Pragya Gupta and Dipankar Pal, "DPL-Based Novel CMOS 1-Trit Ternary Full-Adder," *International Journal of Electronics (IJE), Taylor & Francis*, 2020, vol.108, no.2, pp. 218-236, Print ISSN: 0020-7217 Online ISSN: 1362-3060. DOI: 10.1080/00207217.2020.1789759. Impact Factor: **1.004**.

   http://mjl.clarivate.com/cgi-bin/jrnlst/jlresults.cgi?PC=MASTER&ISSN=*1362-3060

3. **Aloke Saha**, Rahul Pal and Jayanta Ghosh, "Novel Self-Pipelining Approach for Speed-Power Efficient Reliable Binary Multiplication," *Micro and Nanosystems, Bentham Sciene Publication,* 2020, vol.12, no.3, pp. 149-158, ISSN (Print): 1876-4029, ISSN (Online): 1876-4037. DOI: 10.2174/1876402911666190916155445.

4. **Aloke Saha** and Narendra Deo Singh, "Systematic Design Strategy for DPL-based Ternary Logic Circuit," *International Journal of Nanoparticles (IJNP), Inderscience,* 2020, vol. 12, no. 1-2, pp. 3-16, 2020. ISSN online: 1753-2515, ISSN print: 1753-2507. DOI: 10.1504/IJNP.2020.105997.

5. **Aloke Saha** and Dipanakar Pal, "DPL-Based Novel Time Equalized CMOS Ternary-to-Binary Converter, *International Journal of Electronics (IJE), Taylor & Francis*, 2019, vol.107, no.3, pp. 431-443, Print ISSN: 0020-7217 Online ISSN: 1362-3060. DOI: 10.1080/00207217.2019.1661026. Impact Factor: **1.004**.

   http://mjl.clarivate.com/cgi-bin/jrnlst/jlresults.cgi?PC=MASTER&ISSN=*1362-3060

6. **Aloke Saha,** Rahul Pal, Akhilesh G. Naik and Dipankar Pal, "Novel CMOS Multi-bit Counter for Speed-Power Optimization in Multiplier Design," AEU-*Int. J. of Electronics & Communication (IJEC),* Elsevier, 2018, vol. 95, pp. 189-198, ISSN: 1434-8411. DOI: 10.1016/j.aeue.2018.08.015. Impact Factor: **3.183**.

   http://mjl.clarivate.com/cgi-bin/jrnlst/jlresults.cgi?PC=MASTER&ISSN=*1434-8411

7. **Aloke Saha** and Dipankar Pal, "DPL-Based Novel Binary-to-Ternary Converter on CMOS Technology," AEU-*International Journal of Electronics & Communication (IJEC),* Elsevier, 2018, vol. 92, pp. 69-73, ISSN: 1434-8411. DOI: 10.1016/j.aeue.2018.05.020.

   http://mjl.clarivate.com/cgi-bin/jrnlst/jlresults.cgi?PC=MASTER&ISSN=*1434-8411

8. **Aloke Saha,** Sushil Kumar, Debajit Das and Mrinmoy Chakraborty, "LPHS Logic Evaluation on TSMC 0.18µm CMOS Technology**,"** *International Journal of High Speed Electronics & Systems (IJHSES)*, World Scientific, 2017, vol. 26, no. 4, ISSN (print): 0129-1564, ISSN (online): 1793-6438. DOI: 10.1142/S0129156417400249.

9. **Aloke Saha,** Dipankar Pal and Mahesh Chandra, "Benchmarking of DPL Based 8b×8b Novel Wave-Pipelined Multiplier," *Int. J. of Electronics Letters (IJEL),* Taylor & Francis, 2017, vol.5, no.1, pp.115-128, Print ISSN: 2168-1724, Online ISSN: 2168-1732. DOI: 10.1080/21681724.2016.1175031.

10. **Aloke Saha**, Dipankar Pal and Mahesh Chandra, "Low power 6-GHz wave-pipelined 8b×8b multiplier," *IET Circuits, Devices & Systems*, 2013, vol. 7, no. 3, pp. 124-140, Print ISSN: 1751-858X, Online ISSN:1751-8598. DOI: 10.1049/iet-cds.2012.0221.

    http://mjl.clarivate.com/cgi-bin/jrnlst/jlresults.cgi?PC=MASTER&ISSN=*1751-8598

11. Rakesh Kumar Singh, Prerona Sanyal and **Aloke Saha**, "Design of STI, NTI And PTI With Normal Process E-MOSFET on 65nm CMOS Technology," *BCREC Engineering & Science Transaction*, 2020, Vol. 1, Issue 1, pp. 18-23, ISSN: 2582-9068.

Conference:

1. Somashree Chakraborty, Sonali Priya, Tripti Kumari, Saloni Thakur and **Aloke Saha**, "MUX-based Novel 9-trit CMOS Ternary Barrel Shifter," *3rd International Conference on Communication, Devices and Computing* (ICCDC 2021) Springer, 16-17 August 2021, International Conference, Springer. (In press).

2. Rahul Pal, Rakesh Kumar Singh, Jayanta Ghosh and **Aloke Saha**, "Novel 9:1 Ternary Multiplexer on 32nm CMOS Technology," *International Conference on Devices for Integrated Circuits (DevIC-2021)*, *KGEC Kalyani, 19-20* May 2021, International Conference, IEEE, Electronic ISBN:978-1-7281-9955-9, Print on Demand(PoD) ISBN:978-1-7281-9956-6, DOI: 10.1109/DevIC50843.2021.9455836.

3. Rahul Pal, Jayanta Ghosh and **Aloke Saha**, "Novel Self-Pipelining Strategy for Efficient Multiplications," *IEEE International Conference on Devices for Integrated Circuits (IEEE DevIC-2019)*, *KGEC Kalyani,* pp. 298-301, 23-24 March 2019, International Conference, IEEE, Electronic ISBN:978-1-5386-6722-4, Print on Demand(PoD) ISBN:978-1-5386-6723-1, DOI: 10.1109/DEVIC.2019.8783651.

4. Narendra Deo Singh, Rakesh Kumar Singh, Rahul Raj, Shivam Jyoti and **Aloke Saha**, "Novel Approach to Design DPL-based Ternary Logic Circuits," *IEEE Electron Device Kolkata Conference 2018 (IEEE EDKCON-18),* Kolkata, pp.- 631-635, 24-25 November 2018, International Conference, IEEE, Electronic ISBN: 978-1-5386-6415-5, Print on Demand (PoD) ISBN:978-1-5386-6416-2, DOI: 10.1109/EDKCON.2018.8770493

5. **Aloke Saha** and Mrinmoy Chakraborty, "Study on LP-HS Logic for High Performance Digital Applications," *IEEE International Conference on Devices for Integrated Circuits (DevIC-2017)*, *KGEC Kalyani,* pp. 376-379, 23-24 March 2017, International Conference, IEEE, Electronic ISBN:978-1-5090-4724-6, Print on Demand(PoD) ISBN:978-1-5090-4725-3, **DOI:** 10.1109/DEVIC.2017.8073973.

6. **A. Saha,** D. Pal, Mahesh Chandra and M.K. Goswami, "Novel high speed MCML 8-bit by 8-bit multiplier," *IEEE International Conference on Devices & Communications (ICDeCom-11),* BIT Mesra, India, pp. 1-5, 24-25 February 2011, International Conference, IEEE, Electronic ISBN:978-1-4244-9190-2, Print ISBN:978-1-4244-9189-6, CD:978-1-4244-9188-9, DOI: 10.1109/ICDECOM.2011.5738526.

7. Marisha Gautam, Pratik Rajhans, Himanshu Kumar Verma, Ketan Dulwani, Ranojoy Chowdhury, Prerona Sanyal and **Aloke Saha**, "Ternary Middle Value Decoder (T-MVD) on 90nm CMOS Technology," *IEEE National Conference on Emerging Trends on Sustainable Technology and Engineering Applications (NCETSTEA)* 2020, pp. 1-3, 7-8 Feb. 2020, National Conference, IEEE, Electronic ISBN:978-1-7281-4362-0, Print on Demand(PoD) ISBN:978-1-7281-4363-7, DOI: 10.1109/NCETSTEA48365.2020.9119954.

Book Chapter:

1. Rahul Raj, Rakesh Kumar Singh, Narendra Deo Singh, Saubhik Kumar and **Aloke Saha**, "DPL-based Novel 1-trit Ternary Half Subtractor," *vol 602, pp 185-192, Lecture Notes in Electrical Engineering, Springer*, December 2019, Print ISBN: 978-981-15-0828-8, Online ISBN: 978-981-15-0829-5, DOIhttps://doi.org/10.1007/978-981-15-0829-5_18.

Supervision of Ph.D/M.Tech / B.Tech Projects:

Ph.D

1. Mr Rahul Pal (Roll No: 185EC10), Joint Supervisor: **Dr. Aloke Saha** and Dr. Jayanta Ghosh, "Title: Investigations on Low Power Solutions for Digital Circuits", 2018, National Institute of Technology (NIT), Patna (Registered)

M.Tech Thesis

1. Prerona Sanyal (University Roll No. 12013518001), Supervisor: **Dr. Aloke Saha**, "Title: Design of novel Ternary Encryptor and decryptor using DPL for Secure Digital Transmission", 2020.
2. Somnath Maity, Supervisor: **Dr. Aloke Saha**, "Title: Scalable multiplier architecture for low-power high-speed applications", 2014.
3. Charu Hashi Rena (University Roll No. 12020412001), Supervisor: **Dr. Aloke Saha**, "Title: High precision 8-bit square root decoder", 2014.
4. Vikas Kumar (University Roll No. 12020412003), Supervisor: **Dr. Aloke Saha**, "Title: Novel multi input compressors based 8×8 bit parallel multiplier", 2014.
5. Anwesa Sanphui (University Roll No. 12009911007), Supervisor: **Dr. Aloke Saha**, "Title: Design of low power ±0.9V DPCCII- based RMS Detector for low frequency low voltage applications", 2013.
6. Sankalita Pal (University Roll No. 09120099017), Supervisor: **Dr. Aloke Saha**, "Title: High-speed, power-efficient 8-bit square root circuit in TSMC 0.18µm CMOS Technology", 2012.
7. Rahul Pal (University Roll No.12009910017), Supervisor: **Dr. Aloke Saha**, "Title: Novel Self-Pipelined Decomposition based Wallace Tree multiplier for low power application", 2012.
8. Santimoy Mondal (University Roll No. 09120099011), Supervisor: **Dr. Aloke Saha**, "Title: Design of 8b × 8b Multiplier using delay equalisation in 0.18 µm CMOS Technology", 2011.

B.Tech Project

1. Somashree Chakraborty (Univ. Roll. 12000317038) & Sonali Priya(Univ. Roll. 12000317037), Supervisor: **Dr. Aloke Saha**, "Title: Design of 9-Trit Ternary Barrel Shifter on 32nm CMOS Technology**",** 2021.

2. Saloni Thakur (12000317053), Anu Dutta (12000317122) & Rajani Kumari (12000317136), Supervisor: **Dr. Aloke Saha**, "Title: Design of Ternary Half Subtractor with PTL based Ternary 3:1 Multiplexer", 2021.

3. Tripti Kumari (12000317017), Anushka Verma (12000317119) & Anamika (12000317127), Supervisor: **Dr. Aloke Saha**, "Title: Design of Ternary Adder with PTL based Ternary Multiplexer", 2021.

4. Marisha Gautam (12000316089) & Ranojoy Chowdhury (12000316056), Supervisor: **Dr. Aloke Saha**, "Title: Design of Ternary Middle Value Decoder (T-MVD) on CMOS Technology", 2020.

5. Pratik Rajhans (12000316065), Ketan Dulwani (12000316098) & Himanshu Kumar Verma (12000316102), Supervisor: **Dr. Aloke Saha**, "Title: Design of novel 9:1 ternary multiplexer", 2020.

6. Narendra Deo Singh (12000315065) & Shivam Jyoti (12000315098), Supervisor: **Dr. Aloke Saha**, "Title: Novel DPL-based 4-trit Ternary Comparator", 2019.

7. Rakesh Kumar Singh (12000315076) & Pragya Gupta (12000315072), Supervisor: **Dr. Aloke Saha**, "Title: Design of 4-Trit × 4-Trit Pair-Wise Wave pipelined Vedic Ternary Multiplier Using Double Pass Transistor Logic", 2019.

8. Rahul Raj (12000315075) & Saubhik Kumar (12000315093), Supervisor: **Dr. Aloke Saha**, "Title: Novel Ternary Subtractor using Double Pass-transistor Logic (DPL)", 2019.

9. Atul Kumar (12000314019), Dipak Dey (12000314032) & Preetam Kumar (12000314067), Supervisor: **Dr. Aloke Saha**, "Title: Design of DPL based wave pipelined four trit ternary multiplier on TSMC0.18µm CMOS technology", 2018.

10. Md. Naushad (12000314048) & Abhishek Kumar Jha (12000315125), Supervisor: **Dr. Aloke Saha**, "Title: Design of DPL based wave pipelined four trit ternary divider on TSMC 0.18um CMOS technology", 2018.

11. Abhinandan Sharma (12000313002), Abhinav Kumar (12000313003), Arinjoy Poddar (12000313023), Mrinal Bhardwaj (12000313050), Shashwat Kumar (12000313088) & Shubham Kumar Sinha (12000313093), Supervisor: **Dr. Aloke Saha**, "Title: DPL-Based Novel Wave-Pipelined 2:4 Ternary-to-Binary Converter (TBC)", 2017.

12. Ankit Kumar (12000312016), Avinash Kumar (12000312028), Debajit Das (12000313119), Ritesh Kumar Keshri (12000312078) & Sushil Kumar (12000312119), Supervisor: **Dr. Aloke Saha**, "Title: DPL-Based Novel Wave-Pipelined Binary-to-Ternary Converter (BTC)", 2016.

13. Pooja prakasham (Roll: 12000311065), Noor jahan (Roll: 12000311058), Puja dutta (Roll: 12000311071), Nilesh kumar (Roll: 12000311056) & Pratik (Roll: 12000311067), Supervisor: **Dr. Aloke Saha**, "Title: Analysis of LP-HS logic in favor of high performance digital applications", 2015.

14. Abhay Kumar (Roll: 12000311002), Saket Sharma (Roll: 12000311093), Sudhanshu Ranjan (Roll: 12000312136) & Pawan Kumar (Roll: 12000311063), Supervisor: **Dr. Aloke Saha**, "Title: Study on TSPC-F/F for low-power high-speed application", 2015.

15. Md Shahnawaz (Roll: 12000310001), Shipra Kumari (Roll: 12000310020), Aamir Saud Khan (Roll: 12000310027) & Mugdha Kashyap (Roll: 12000310052), Supervisor: **Dr. Aloke Saha**, "Title: Design and analysis of different 3:2 compressor circuits to compare speed-power performance on TSMC 0.18µm CMOS technology at 25°C temperature", 2014.

16. Ajit Prakash (Roll: 09120003039), Rajib Dey (Roll: 09120003079), Rahul Kumar (Roll: 09120003078) & Mayank (Roll: 09120003068), Supervisor: **Dr. Aloke Saha**, "Title: Design of low-power low-skew clock generator for time equalized applications", 2013.

Participation in seminar/conference/symposium/workshop/discussion meeting

S. No.	From	To	Organized by	Name of the event Course
1.	27/02/2021	27/02/2021	R&D Cell, Dr. B. C. Roy Engineering College, Durgapur	Journey from Vacuum Tube to Carbon Nanotube
2.	18/9/2020	20/9/2020	Electronics and Communication Engineering Department, BCREC and IEEE student branch BCREC	Trends of Modern Communication Engineering Systems
3.	30.09.2020	30.09.2020	Sanjeevani....Life beyond Cancer	Eradicating Cancer & Step Towards Healthy Lifestyle.
4.	22.08.2019	22.08.2019	IEEE Student Branch & IEI Student Chapter, BCREC	Seminar on "Teaching and Learning Skill Development"
5.	23.03.2017	24.03.2017	Kalyani Govt. Engineering College, Kalyani	IEEE Int. Conf. on Devices for Integrated Circuits (DevIC-2017)
6.	04.11.2015	04.11.2015	R &D Centre, Dr. B. C. Roy Engineering College	Seminar on "Advances in Nano-Satellite Technology"
7.	24.02.2011	25.02.2011	BIT Mesra	International Conference on Devices & Communications (ICDeCom11) 2011
8.	20.07.2009	24.07.2009	Bengal College of Engineering & Technology, Durgapur	NEN Foundation course
9.	04.01.2009	10.01.2009	Bengal Engineering & Science University (BESU) Shibpur	National workshop on Recent Trends in VLSI Design and Microelectronics
10.	14.02.2008	15.02.2008	Cadence Design Systems (I) Pvt. Ltd.	Cadence Tools Training
11.	05.12.2007	06.12.2007	NIT Rourkela	Workshop on Embedded System & DSP in VLSI
12.	11.06.2006	02.07.2006	Red Hat India Pvt. Ltd.	Training on "Red Hat Linux (RH033)"

Participation in faculty development programmes

Sl. No.	Name of the faculty development programmes	Online / Face-to-face	From	To	Duration	Organized by
1.	ASIC- Physical Design and Verification using Mentor toolset	Online	07.05.2020	09.05.2020	3 days	Sandeepani School of Embedded System Design, Bangalore in collaboration with Xilinx and Corel Technologies
2.	Hands on training on "Full-custom VLSI Design using Mentor Graphics" by CorEL Technologies (I) Pvt. Ltd. Bengaluru	Face-to-face	15.05.2019	17.05.2019	3 days	ECE Department, Dr. B. C. Roy Engineering College, Durgapur

Organization of events (Dr. B. C. Roy Engineering College)

Sl. No.	Name of the event	From	To	Responsibility
1.	National Conference on Emerging Trends on Sustainable Technology and Engineering Applications (NCETSTEA) 2020	07.02.2020	08.02.2020	Financial Co-chair
2.	Hands on training on "Full-custom VLSI Design using Mentor Graphics" by CorEL Technologies (I) Pvt. Ltd. Bengaluru	15.05.2019	17.05.2019	Organizing Committee Member
3.	Microwave Engineering & Applications (MEA-2015)	14.03.2015	15.03.2015	Organizing Committee Member

Participation in administrative committees (selected)

- M.tech (Microelectronics Engineering) Course Co-ordinator from year 2012 to year 2014

Project Ideas Submitted to Govt. Agencies/ On-going Projects / Research Ideas under preparation & execution

Sl. No.	Title	Type	Coordinator	Submitted to	Submitted on	Present Status
1.	Up-gradation/Modernization of "*VLSI Design & Research*" Laboratory (Phase-II) together with Mentor-Graphics License renewal	MODROB	Dr. Aloke Saha & Dr. Tribeni Prasad Banerjee	AICTE	28.01.2021	Under Review
2.	FDP on "Microelectronics and VLSI Technology"	FDP	Dr. Aloke Saha	AICTE	21.12.2019	Not Recommended

Membership of professional bodies: IEEE, IETE, IEI, CSI, MGMI etc.

- Member IEEE (Since 2015): Member Number 93689053

I hereby declare that all the statements made above are true, complete and correct to the best of my knowledge and belief.

Dr. Aloke Saha
Assistant Professor,
Department of ECE,
Dr. B. C. Roy Engineering College, Durgapur