2024 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON) | 979-8-3503-7464-3/24/$31.00 ©2024 IEEE | DOI: 10.1109/EDKCON62339.2024.10870766

Proceedings of

2024 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)

30th November – 1st December, 2024, Kolkata, West Bengal, India

Place: Fairfield by Marriott, New Town, Rajarhat, Kolkata, India

Organized by

IEEE EDS Kolkata Chapter

Novel Sign-Magnitude Binary to Balanced-Ternary Encoder on Basys3 Artix7 FPGA

Ashishit Anurag Daniel Tigga
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
ashishitdaniel@ gmail.com

Nishit Bayen
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
nishitbayen2021@ gmail.com

Suman Gorai
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
sumangorai033@ gmail.com

Pradipta Sarkar
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
pradipta.sarkar@ bcrec.ac.in

Anup Kumar Das
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
anupkumardgp@ gmail.com

Aloke Saha
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
saha81 @gmail.com

2024 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON) | 979-8-3503-7464-3/24/$31.00 ©2024 IEEE | DOI: 10.1109/EDKCON62339.2024.10870764

***Abstract*—In the realm of digital systems, binary representation has been the predominant method for data encoding and processing. However, alternative numbering systems such as ternary (base-3) have gained considerable attention over binary due to its ability to reduce interconnect complexity for identical data processing. Balanced ternary offer several advantages over unbalanced ternary in certain applications. This report outlines novel binary to balanced ternary encoder that accepts 9-bit sign-magnitude binary data (-255 to +255) and generates 6-trit ternary equivalent in BET (Binary Encoded Ternary) format. The theoretical analysis is explained and the corresponding verilog code is simulated using Xilinx-vivado software to validate the idea. After behavioral simulation, the circuit is synthesized and implemented for the target device Xilinx Basys3 Artix-7 FPGA: XC7A35T-1CPG236C. Post implementation bit stream is downloaded on to the target FPGA for prototype verification.**

***Keywords*—** *Balanced Ternary, Basys3 Artix7 FPGA, Binary System, FPGA Design Flow, Verilog-HDL.*

I. INTRODUCTION

Two stable state (ON/OFF) of practical solid-state device makes binary-system a default choice to implement digital circuits/systems from the beginning [1-2]. Steady advancement in scaling technology calls for growing function-density in a single monolithic-IC towards development of low-power sophisticated smart digital system for next generation IOT, Artificial Intelligence, cryptography and so on. However, associated interconnect complexity makes well established binary-system less interesting in current scenario and directed researcher to reinvestigate alternative number system to deal with the related concern [3-4]. Study on MVL establishes ternary (base-3) as the most relevant number system to represent digital data from long back [5], however it was ignored mainly because of practical implementation constraints. Ternary is once again at the centre of attraction in recent research [6-12] due to its capability to bring-down interconnect complexity by using less component block for identical data processing as compared to its binary counterpart and also being closure to natural base-e (i.e. "e" = 2.718), can offer optimum accuracy [12-14] .

Ternary uses three-levels of signaling that can be represented either by the set {0, 1, 2} (i.e. unbalanced ternary) [1] or by the set {-1, 0, 1} (i.e. balanced ternary) [12]. In 2014, S. Ahmad et. al [15] claimed balanced ternary as the most suitable number system to enhance circuit performance in favor of modern digital computing. Two years before in 2012, M. Eaton [16] applied balanced ternary to propose 1-trit ternary ALU to apply for cybernetic intelligence. In the next year 2013 a balanced ternary adder was proposed with the help of memristor [17]. Later in the year 2015, B. Parhami [18] explored the merit of balanced ternary scheme with respect to truncated ternary multiplication. B.Cambou et. al in 2018 [19] suggested balanced ternary for IOT security applications. Recently in 2019, the superiority of balanced ternary over unbalanced ternary was investigated and presented by M. Toulabinejad et. al [12].

Since, existing systems are compatible with binary system, to exploit the merits of balanced-ternary, binary-to-balanced ternary encoder serve as an essential data-path building block. With aforesaid interest, F.-Q. Li et. al proposed binary-to-ternary converter with Josephson strategy in 1995 [20]. However, the strategy is unfit to cope-up with current demand. Recently in the year 2018, Md. M. Rahman et. al [21] proposed a combined balanced ternary system to deal with the complexity of the binary to balanced ternary conversion method. The idea in [21] does not produce true balanced-ternary equivalent. With the best of our understanding no hardware implementation strategy for binary-to-balanced ternary conversion is available in open literature and that has been motivated the present work.

Current study unfolds a novel idea to convert sign-magnitude binary input into its balanced ternary equivalent. Proposed idea is validated by constructing 9-bit:6-trit binary to balanced ternary encoder in verilog-HDL, Synthesizing the design after behavioural simulation and implementing on Xilinx Basys3 Artix-7 FPGA: XC7A35T-1CPG236C for prototype verification. The 9-bit input for the encoder is in sign-magnitude form that considers the decimal value -255 to +255 and the corresponding ternary outcome is presented in its BET (Binary Encoded Ternary) form. Each trit output in BET is represented with 2-bits (i.e. "00" for trit value "0", "10" for trit value "1" and "01" for trit value "T"). The "T" denotes "-1" in our system. The circuit performance is recorded.

The ordering of rest of the sections are follows: section-II discusses the proposed conversion strategy for sign-magnitude binary input to its balanced ternary equivalent.