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Novel Low-PDP CMOS Double-base Comparator

Rahul Pal
Dept. of ECE
NIT, Patna
Patna,India
rahulmail08@ gmail.com

Jayanta Ghosh
Dept. of ECE
NIT, Patna
Patna,India
jghosh@ nitp.ac.in

Aloke Saha
Dept. of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
saha81@ gmail.com

***Abstract*— Double-base system offer redundancy and is exploited here to propose new low-PDP (Power Delay Product) double-base comparator to mitigate the power-delay hazards of conventional single-base comparator. Proposed 3-step design strategy is illustrated by designing [2×2] double-base comparator on 32n-meter usual Complementary-MOS Technology with 900m-Volt supply at nominal temperature (27°C). After transient validation with every-probable custom test inputs the worst-case power-delay response is tabulated. Proposed [2×2] double-base comparator is then compared with most relevant binary and ternary counterpart available in open literature to benchmark. As per study the proposed double base comparator can offer of at least 27% power-cut as compared to its most competitive traditional counterpart.**

Keywords*— *Double-base Comparator, Double-base Number System (DBNS), Power-dissipation, Single-base Comparator, T-Spice Simulation

I. INTRODUCTION

The Challenges on low-power solution for digital circuits have been increasing due to high demand for portable sophisticated (i.e. AI/IOT) devices in recent time [1-5]. Digital comparator [3] is considered as a major data-path-component towards digital data processing and hence, low-PDP comparator is always on high demand for portable sophisticated smart system development in present scenario. Conventional single-base binary comparator loses its reliability due to large interconnect complexity. Carrying more information with less number of communicating channel makes multi-valued ternary comparator a feasible alternative to binary counterpart [2]. However, complexity of primary logic cell is the matter of concern [2]. More efficient strategy need to be developed to exploit full advantage of ternary system.

In contrary, the Double-base Number System (DBNS) [6-17] offer redundancy and associated parallelism. This makes the DBNS a candidate of choice to reduce the carry propagation and accordingly to improve the operating speed. However, power optimization with double-base computing is an open challenge due to its redundancy property [11]. With clever strategy the double-base comparator can offer better solution for speed-power performance for identical data processing as compared to its single-base counterpart [7].

The work investigates novel low PDP Double base comparator for AI/IOT enabled portable electronic system. An illustrative [2×2] double-base comparator using 32nm typical Complementary-MOS tech. file with BSI-Model4 model-parameters and 900-mVolt source at 27°-Centigrade is designed. Working of proposed DB-Comparator is checked through transient simulations applying every-probable input combinations. Proposed comparator is compared with most relevant equivalent single-base comparator available in open literature to benchmark.

The other sections of the manuscript are structured as follows: Sec.-two is responsible to explore the proposed circuit strategy for double-base comparator. The circuit design, simulation and benchmarking is disclosed in Sec.-three. Sec.-four is dedicated for the concluding remarks.

II. PROPOSED DOUBLE-BASE COMPARATOR

The block-level process-flow structure of proposed double-base comparator is illustrated in Fig.1. Activity of each block in Fig.1 is explained next with respect to proposed [2×2] double-base comparator.

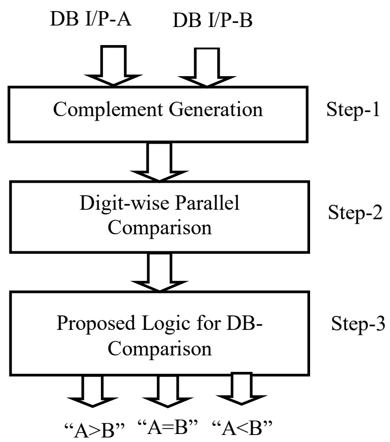

Fig. 1. Proposed Strategy for DB-Comparison

TABLE I. DB INPUT-A

Base-3 \ Base-2	2^0	2^1	
3^0	A_{00}	A_{01}	R-0
3^1	A_{10}	A_{11}	R-1
	C-0	C-1	

TABLE II. DB INPUT-B

Base-3 \ Base-2	2^0	2^1	
3^0	B_{00}	B_{01}	R-0
3^1	B_{10}	B_{11}	R-1
	C-0	C-1	

In Fig.1 "A" and "B" are the two [2×2] double-base input applied to the comparator with coefficients "A_{00}, A_{01}, A_{10}, A_{11}" (Table-I) and "B_{00}, B_{01}, B_{10}, B_{11}" (Table-II) respectively. Proposed 3-step strategy to compare "A" and "B" is explained below: