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Power Efficient Novel CMOS Double-base to Binary Encoder (DBE)

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Abstract*—Double-base number system can be promising substitute to usual single-base system owing to its redundancy property. Binary is the well-established number system in digital domain and hence, efficient double-base to binary encoding is utmost essential to exploit the advantage of double-base system. In this paper a novel low power Double-base (binary & ternary) to Binary (base-2) Encoder (DBE) based on CMOS logic style is explored. The proposed two steps strategy consists of generating unary equivalent of double-base input by applying novel idea first and encoding unary result into binary next with conventional approach. The traditional CMOS Inverter is exploited to invert the double-base coefficient required for unary-generator. An illustrative [3×3]:4-bit DBE-circuit is optimized on 32n-meter typical Complementary-MOS technology considering BSIM4 Device parameters with 900mili-V supply at 27°-Centigrade nominal temperature. The proposed DBE has been checked using T-Spice transient-simulations considering every probable test inputs. The layout of the circuit is done on 32n-meter SPDM process-node and the circuit characteristic with extracted parasitic is compared with most relevant counterpart to benchmark. The circuit performance with load variation is measured and recorded.

Keywords*— *Double-base system, Logic Gates, Single-base system, Unary System, Power Dissipation

I. INTRODUCTION

Increasing demand for multitasking smart system makes the speed-power efficiency as a major concern in present scenario [1-2]. Traditionally digital circuits are being designed with base-2 or binary logic [1-3]. Large interconnect complexity associated with conventional single-base binary number system towards sophisticated smart system development is a major bottleneck to the circuit/system designer. Some recent study shows that the radix-3 (ternary) system can offer possible solution but the complexity at basic logic-level is the matter of worry and need some novel solution to discover [4-8].

Technological advancement and need of higher computing power in digital domain call for architectural modification in conventional (single-base) approach. As a result, 2-dimensional double-base system becomes attractive due to its redundancy, parallelism as well as sharpness properties [9-25]. This can potentially reduce the circuit complexity and hence, can improve overall speed-power-area efficiency. Double-base logic replaces classical single bases logic by accommodating two bases commonly base-2 (binary) & base-3 (ternary). Encoding binary data into its double-base equivalent and the vice-versa is a crucial task to exploit computational advantage of double-base system. This paper deals with double-base to binary encoding. Existing strategies in this regard are highly iterative and power inefficient.

Current work discloses a novel 2-step design strategy to encode the double base input into its binary equivalent using binary logic cells. The circuit operation is elaborated with respect to [3×3]:4 double-base to binary encoding and can be utilized to present any higher order DBE. Front-end design and optimization is done using Tanner EDA S-Edit. After validation through T-Spice simulation the layout on 32n-meter SPDM Complementary-MOS process-node with 900mili-V supply at 27°-Centigrade is done. Next, all the Design-Rules as well as one-to-one correspondence between Layout and Schematic are checked. Post-layout characteristics with extracted parasitic is evaluated and the result is compared to benchmark.

The other portions of this manuscript are structured as follows: Second-Section describes the novel double-base to binary conversion strategy. Circuit design, simulation and benchmarking study is presented in third-Section. The fourth-section is dedicated for conclusion.

II. NOVEL DOUBLE BASE TO BINARY ENCODER

In proposed double-base to binary encoding, the double-base input to the system is transformed into its unary corresponding first and encoded next to 4-bit binary output. To understand better, consider a 3×3 double-base number "A" with coefficient matrix presented in Table-I. The positional coefficients of "A" are denoted by A_{xy} with positional weight 3^x2^y (x^{th} row, y^{th} column) in Table-I. The double-base system carries redundancy property (more than one representation is possible for the same value) and the study [14] shows the optimum performance from double system can be achieved if the number is represented with minimum number of one in the coefficient matrix. In present work, the double base number is optimized to have optimum number of ones in the coefficient matrix before converting into unary equivalent.

TABLE I. A 3×3 DOUBLE-BASE COEFFICIENT TABLE

Base-2 / Base-3	2^0	2^1	2^2	
3^0	A_{00}	A_{01}	A_{02}	R-0
3^1	A_{10}	A_{11}	A_{12}	R-1
3^2	A_{20}	A_{21}	A_{22}	R-2
	C-0	C-1	C-2	