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# Low-PDP 7:3-Counter with Novel Multi-threshold 2:1-Multiplexer

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**Abstract**—Current endeavour unfolds a clever design strategy to achieve low-PDP 7:3-counter using novel multi-threshold 2:1-Multiplexer for efficient multiplication. The idea is verified by constructing gate-level circuit with DSCH3.1 first and corresponding transistor-level circuit is designed next on 45nm PDK with BSIM4 technology parameters using Tanner EDA S-Edit. The 1100m-V is the main supply for the design and is excited with every possible custom bit-pattern using v-bit input source of Tanner-EDA to validate. The layout of proposed counter is constructed with 45-nm SPDM CMOS process technology and is evaluated through post-layout transient simulation in all three design corner (i.e. TT, SS and FF) applying 10k random test-patterns at room temperature. The PDP (Power-Delay-Product) is the crucial FOM for digital circuit and that has been measured and benchmarked with some recent competitive designs under same sets of test-pattern@125MHz data rate and in identical operating environment.

**Keywords**—Multi-bit Counter, Multi-threshold MOSFET, MOSFET Pass-Characteristics, Power-Delay-Product (PDP), 2:1 Multiplexer

## I. INTRODUCTION

Ever-rising computational complexity of digital signal/image/video processing towards modern IOT/AI-based sophisticated system development has shaped the need for highly efficient high-speed multiplier as a critical datapath building-block [1-7]. Power-Delay efficiency of a CC-parallel multiplier depends mostly on its technique to compress the Partial Products [8]. Some of the recent study [6-7, 9-10] shows that the clever use of multi-bit counter/adder in PPR-stage can essentially enhance the performance of multiplier circuit. However, dealing with internal circuit complexity and carry-propagation of multi-bit counter is an open challenge and is the prime focus in present scenario.

In this context, S. Mehrabi et. al [11] analyzed and compared two different architecture (i.e. MUX/XOR-based and conventional) for 6:3 and 7:3-counter in terms of speed-power performance on 32nm CNTFET. Later in 2014, M. Ghasemzadeh et. al [12] claimed a glitch reduction strategy for 7:3 counter to attain overall power reduction of the circuit. A. Saha et. al in 2018 [9] proposed delay equalized multi-bit counter exploiting novel grouping and optimization strategy for efficient multiplication. In June-2019 novel current-mode 7:3 counter is proposed by S. Ghafari et. al

[13] in favor of high-speed applications. In the same year 2019, T. Satish et. al [14] disclosed a novel multi-bit counter architecture with binary NAND logic. Further in October 2020 [15], S. H. Bandarupalli et. al investigated and explored optimum performance of 7:3-counter using Full Swing XOR circuit. Next, an efficient multi-bit counter architecture was proposed in January 2021 [6] for high-speed multiplication. A sorting network based fast binary counter is proposed by W. Guo et. al in June 2021 [16]. Further in May 2022, low-power, area efficient 7:3-counter was proposed by G. R. Chowdary et. al [17]. Most recently in May 2024 [7], B. Mukherjee proposed novel low-power 7:3-counter using hybrid Full-Adder circuit.

Present study aims to disclose a clever idea to reduce the Power-Delay-Product (PDP) of 7:3-counter using novel multi-threshold 2:1-multiplexer. Low, Typical and High threshold MOSFETs are strategically placed and sized to optimize the performance of proposed multi-threshold 2:1-multiplexer first and is exploited next to propose novel speed-power efficient 7:3-counter. The logic verification of proposed 7:3-counter is done with DSCH3.1 software and the corresponding MOS-level circuit is designed on 45nm technology node with 1100m-V source-supply at room temperature using Tanner Schematic-Editor. Custom test pattern is generated through v-bit input source for transient validation in SS, TT and FF design corner. Layout of the counter is constructed with 45-nm SPDM process node and the post-layout power-delay characteristic is compared with some most recent competitive counterpart under identical operating condition (TT-condition) and 125MHz input to benchmark.

Further sections of the manuscript are arranged as follows: The design idea of proposed 7:3-counter using novel multi-threshold MOSFET and its working is discussed in 2<sup>nd</sup> Section of the manuscript. The 3<sup>rd</sup> Section deals with design, evaluation and benchmarking of proposed counter with competitive counterpart. The manuscript is concluded in Section-4.

## II. EASE PROPOSED 7:3 COUNTER WITH NOVEL MULTIPLEXER

The block-level data-propagation structure of proposed 7:3-counter is depicted in Fig.1. The X and M-block in Fig.1 are stands for 2-input XOR and 2:1-Multiplexer circuit respectively. The term “sel” denotes the selection input for