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Novel Sign-Magnitude Binary to Balanced-Ternary Encoder on Basys3 Artix7 FPGA

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Abstract:
In the realm of digital systems, binary representation has been the predominant method for data encoding and processing. However, alternative numbering systems such as ternary (base-3) have gained considerable attention over binary due to its ability to reduce interconnect complexity for identical data processing. Balanced ternary offer several advantages over unbalanced ternary in certain applications. This report outlines novel binary to balanced ternary encoder that accepts 9-bit sign-magnitude binary data (-255 to +255) and generates 6-trit ternary equivalent in BET (Binary Encoded Ternary) format. The theoretical analysis is explained and the corresponding verilog code is simulated using Xilinx-vivado software to validate the idea. After behavioral simulation, the circuit is synthesized and implemented for the target device Xilinx Basys3 Artix-7 FPGA: XC7 A35T -1 CPG236C. Post implementation bit stream is downloaded on to the target FPGA for prototype verification.

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I. Introduction

Two stable state (ON/OFF) of practical solid-state device makes binary-system a default choice to implement digital circuits/systems from the beginning [1]–[2]. Steady advancement in scaling technology calls for growing function-density in a single monolithic-IC towards development of low-power sophisticated smart digital system for next generation IOT, Artificial Intelligence, cryptography and so on. However, associated interconnect complexity makes well established binary-system less interesting in current scenario and directed researcher to reinvestigate alternative number system to deal with the

MVL establishes ternary (base-3) as the most relevant number system to represent digital data from long back [5], however it was ignored mainly because of practical implementation constraints. Ternary is once again at the centre of attraction in recent research [6]–[12] due to its capability to bring-down interconnect complexity by using less component block for identical data processing as compared to its binary counterpart and also being closure to natural base-e (i.e. "e" = 2.718), can

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