

Table of Contents

Paper ID	Paper Title	Page No.
Welcome message from General Chair and General Co-Chair, EDKCON 2024		
1	Investigation of Analog and Digital Performance for Gallium-Arsenide GS GAA FETs. <i>Sneha Singh, Shuvra Jyoti Bose, Abhishek Kumar and Rudra Dhar</i>	1-6
2	Reliability Study of Interface Traps in Gate-All-Around Tunnel FET: A TCAD Simulation Approach <i>Rittik Ghosh, A.Provias, Tathagata Sau, Pragya, Saheli Sarkhel, Priyanka Saha</i>	7-10
3	Theoretical Study of Optoelectronic Nanoparticles Optical Absorption Enhancement <i>Subhamoy Singha Roy, Spandan Karfa, Subham Sharma, Subha Ghosh</i>	11-14
4	Examining the Effect of Size-Dimensional Nanoparticles on Susceptibilities in Two Dimension (2D) <i>Subhamoy Singha Roy, Spandan Karfa, Subham Sharma, Suva Ghosh</i>	15-18
5	Nonlinear Molecular Quantum Dynamics in an Entirely Nonhomogeneous DNA Chain Voltage <i>Subhamoy Singha Roy, Spandan Karfa, Subham Sharma, Suva Ghosh</i>	19-22
6	Comparative Study of Performance Analysis on Secure DSSS Multiuser Detection Under Near-Far Environment <i>Tanajit Manna, Mohankumar N, Dhrubojyoti Banerjee, Shibabrata Mukherjee, Bidrohi Bhattacharjee and Heranmoy Maity</i>	23-28
7	ASIC Flow Implementation on a 32-bit RISC-V Processor using Cadence <i>Mohammed Abdul Raheem, Mohammed Sabir Hussain, and Pathan Rehman Ahmed Khan</i>	29-33
8	Integration of Metallic Moth-Eye Nanostructures for Enhanced Photovoltaic Efficiency in All-Inorganic Perovskite Solar Cells <i>Swagata Bankura and Abhijit Biswas</i>	34-38
9	Study of Three-Subband Electron Mobility in AlGaAs based Semi-Non-Square Quantum Well Structures	39-42

	<i>Narayan Sahoo and Ajit Sahu</i>	
10	Horticulture 4.0: Transforming Agriculture with IoT-Based Need-Specific Irrigation <i>Dushyant Kumar Singh, Reena Chandel and Simerjit Kaur</i>	43-46
11	Systematic Optimization of InBi₂S₄Cl Absorber Layer in Perovskite Solar Cells for Enhanced Photovoltaic Performance <i>Nikhil Shrivastav, Sagar Bhattarai, Jaya Madan, Haider Alabdeli and Rahul Pandey</i>	47-50
12	Bandwidth Improvement of Slits-Slots with DGS Circular Patch Antenna for Wireless Communication <i>Neeru Kashyap, Shikha Verma, Archana Sandhu, Anukriti Sharma and Meenakshi</i>	51-55
13	Comparative Analysis of Power Consumption and Transistor Current for 6T And 9T SRAM <i>Kaushal Kumar, Abhay Tyagi, YashRaj Lata, Vinay Kumar, Ajay Kumar and Aditya Jain</i>	56-60
14	Design of T-shape Tunnel FET with Enhanced Drain current Characteristics at 30nm Technology <i>Ashutosh Yadav, Sweta Chander, Suman Lata Tripathi and Sanjeet Kumar Sinha</i>	61-66
15	Asymmetrically doping dependent Nonlinear Electron Mobility in In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As wide quantum well MODFET structure <i>Sangita Panda, Manoranjan Pradhan, Trinath Sahu and Ajit Kumar Panda</i>	67-71
16	Performance Analysis Of Magnitude Comparator Using An Adiabatic Technique <i>Dharma Teja Lanka, Veera Krishna Badisa, Surya Prakash Devarapalli and Gopi Chand Chinthakayala</i>	72-76
17	Performance Analysis of Biosensor Based on Inverted T shaped Junctionless FinFET <i>Shekhar Verma, Suman Lata Tripathi, Vishal Narula, Nikhil Nikhil and Balwinder Raj</i>	77-82
18	Predictive Modeling for Bandgap Tuning in Perovskite Solar Cells using Machine Learning <i>Dipayan Chatterjee, Suman Panja, Swarupa Das, Sudeshna Kundu, Sowradeep Pal and Kanishka Majumder</i>	83-88
19	An Integrated Framework for Real-time Analysis and Observability of Wireless Sensor Data Using AWS Edge Service Capabilities <i>Saranga Mohan and Sunita Panda</i>	89-94
20	Study the improved efficiency of the Lead-Free CsSnI₃ Perovskite Solar Cells with variation of absorber layer in SCAPS-1D <i>Arijit Kumar Barik, Himadri Sekhar Das, Sudipta Banerjee, Heranmoy Maity, Santanu Mishra and Mousam Chatterjee</i>	95-98
21	Advanced Gas Sensor Design: A Machine Learning Perspective on Photonic Crystals <i>Debjyoti Karmakar, Joydip Saw, Debashis Modak, Subhajit Pramanick, Suman Pal and Kanishka Majumder</i>	99-104
22	Hardware Implementation of Two level Authentication Algorithm using Cryptography with Steganography for Text-Image Security	105-110

	<i>Poulomi Ghosh, Sudip Ghosh and Hafizur Rahaman</i>	
23	Investigation of FinFET with multi-channel structures on device characteristics	111-116
	<i>Archana Singh, Manish Verma and Dhandapani Vaithyanathan</i>	
24	DC Analysis of T shape gate, L shape gate, Y shape gate, Field-plate gate AlGaN/GaN based HEMT	117-120
	<i>Lakhmikanta Mishra, G. N. Dash and Manasa Ranjan Jena</i>	
25	Chaotic Image encryption scheme implemented in FPGA for security enhance	121-125
	<i>Pradipta Sarkar, Anup Kumar Das and Alope Saha</i>	
26	A Novel ASK Reversible Gate and Its Implementation in Ripple Carry Adder Design	126-131
	<i>Aruru Sai Kumar, Pokala Santhosh, Neelima Nimmagadda, Barama Veda Harshitha, D Suvarna Aishwarya Lakshmi and Katkam Shashi Vardhan</i>	
27	Securing the Future of Communication with Quantum Cryptography	132-137
	<i>Parna Kundu, Sudipta Banerjee, Mousam Chatterjee, Himadri Sekhar Das, Aritra Bhowmik and Heranmoy Maity</i>	
28	Classifying the Tongue Contours for Assistive Devices	138-142
	<i>Dasari Lakshmi Prasanna, Suman Lata Tripathi and Inung Wijayanto</i>	
29	Performance of HfO₂ on High Electron Mobility Transistor Compatible for Microwave Applications	143-147
	<i>Swati Dhondiram Jadhav and Aboo Bakar Khan</i>	
30	Enhancing Biosensing Sensitivity through Simulation-Based Study of N⁺ Pocket Doped Vertical NC-TFET	148-153
	<i>Raj Kumar, Girdhar Gopal, Rajendra Mitharwal and Tarun Varma</i>	
31	Novel Sign-Magnitude Binary to Balanced-Ternary Encoder on Basys3 Artix7 FPGA	154-157
	<i>Ashishit Anurag Daniel Tigga, Nishit Bayen, Suman Gorai, Pradipta Sarkar, Anup Das and Alope Saha</i>	
32	Application of Machine Learning Approaches for Power Estimation of Digital VLSI Circuits at Register Transfer Level	158-161
	<i>Chinmay Parmar and Manish I. Patel</i>	
33	Improved Deepmaxoutmodel for Disease Prediction in Healthcare IoT Cloud System	162-167
	<i>Preetha Pandu and A Packialatha</i>	
34	An IoT-based Hardware System for Road Accident Detection and Notification using CNN-LSTM Algorithm	168-173
	<i>Tanusree Chatterjee, Shibasish Dalui, Sanjib Roy, Rituraj Debnath and Avijit Mondal</i>	
35	Design and FPGA Implementation of an Efficient Squarer Circuit Using Reversible Logic	174-178
	<i>Mihir Lal Saha, Debjit Roy, Agnik Maity, Antarik Sinha, Mili Sarkar and Amitava Ghosh</i>	
36	Unveiling Mental Stress: Examining the Impact on College Students' Well-being Using Machine Learning Based Solutions	179-184

	<i>Kanak Kumar, Anshul Verma, Pradeepika Verma and Suman Lata Tripathi</i>	
37	Advancing Solar Cell Efficiency: Performance Insights into Low Lead CsPb_{0.625}Zn_{0.375}I₂Cl Perovskite Solar Cell	185-189
	<i>Navdeep kaur, Jaya Madan and Rahul Pandey</i>	
38	Doping Dependent Electron Transport Mobility in Al_{0.3}Ga_{0.7}As/In_{0.15}Ga_{0.85}As Double Quantum Well Field Effect Transistor Structure	190-194
	<i>Narayan Sahoo, Ajit Sahu and Ram Chandra Swain</i>	
39	Modulation of I-V Characteristics in U-Shaped Armchair Graphene Nanoribbon-based Tunnel Diode	195-198
	<i>Narayan Sahoo, Simran Patra, Ajit Sahu, Madhusudan Mishra, and Deepak K. Naik</i>	
40	FPGA-BASED IMPLEMENTATION OF LIGHTWEIGHT BLOCK CIPHERS	199-204
	<i>Koyel Naskar</i>	
41	NavIC Galileo long distance RTK positioning performance	205-208
	<i>Somnath Mahato, Vijai Kumar, Abhishek Singh, Divyesh Deshpande, Anjit Anjan and Ashim Kumar Mitra</i>	
42	Temperature-based Routing Protocols for Wireless Body Area Networks (WBANs) : A Comparative Analysis	209-214
	<i>Swati Goel, Kalpna Guleria and Surya Narayan Panda</i>	
43	Performance Analysis of a Heterojunction Dual Gate Ferroelectric Tunnel FET with variation of Gate Stack Dielectric combination	215-219
	<i>Shib Sankar Das, Sudipta Ghosh and Subir Kumar Sarkar</i>	
44	Impact of Hole Gas in O₂ sensing Applications in Ge Core Si Shell Nanowires: Quantum Simulation Study	220-224
	<i>Sharmistha Shee Kanrar, Komal Kumari, Abir Jana, Bhaskar Gupta, and Subir Kumar Sarkar</i>	
45	Performance Analysis of Multiplexer based Ternary Multiplier Designed Using FinFET models	225-229
	<i>Mohit Kumar Goel and Kulbhushan Sharma</i>	
46	Time- Dependent Eikonal Solution using Physics- Informed Neural Networks	230-235
	<i>Indrajit Das, Debjit Das, Abheepsa Bhattacharya, Papiya Debnath, Subhrapratim Nath and Manash Chanda</i>	
47	Solution of Allen – Cahn equation using Physics – Informed Neural Networks	236-240
	<i>Indrajit Das, Debjit Das, Abheepsa Bhattacharya, Papiya Debnath, Subhrapratim Nath and Manash Chanda</i>	
48	Analysis of Tripple-Step Gate Field Plated AlGa_N/Ga_N Based HEMT for High Power Applications	241-245

	<i>Sahil Kumar, Utkarsh, Swapnendu, Harsh Ranjan, Shashank Kumar Dubey, Soumak Nandi, Mukesh Kumar and Aminul Islam</i>	
49	Study on Deep Learning based Classification Models for Multiple Sclerosis in MRI Datasets <i>Kamarujjaman, Srirupa Das, Joy Samadder and Jadav Chandra Das</i>	246-251
50	Fringing Effects in a Capacitive Micromachined Ultrasonic Transducer with a SiC actuation Layer insulated by High dielectric material <i>Sk.Sohel Ahamed, Moumita pal, Pritam Chakraborty, Biswarup Neogi, Niladri Maity and Reshmi Das</i>	252-257
51	Enhancing Public Health Measures with AI and MobilenetV2 for Face Mask Detection <i>Mangal Patil, Prajakta Naregalkar, Aparna Patil, Jyoti Morbale, Saloni Aggarwal, T. Sneetha Reddy, Divya Sharma, Nikhat Anjum, Raushan Kumar, Rahul Kumar Raj and Vijay Nath</i>	258-263
52	Lateral Straggle Based Interface Trap Sensitivity in n-p-n SOI Double Gate TFETs <i>Deepjyoti Deb, Saurav Nath, Prachuryya Das, Rupam Goswami and Ratul Baruah</i>	264-268
53	Phase Correction using single Current feedback amplifier <i>Rimpi Datta, Koushick Mathur, P. Venkateswaran and R. Nandi</i>	269-272
54	Development of IoT based n-ZnO/p-rGO Nanohybrid H2 Sensor Node <i>Swapan Das, Sunipa Roy, Chandan Kumar Sarkar, Rup Pratim Ghatak, Tanisa Halder and Bishwarup Choudhury</i>	273-278
55	Study of thermal noise in InAs_xSb_{1-x} UTB MOS under sub-100 nm range <i>Palasri Dhar, Sunipa Roy, Swagata Bhattacharjee and Sandipta Paul</i>	279-282
56	Investigations on novel Dual Metal Gate-Vertical C-channel Nanosheet FET with fT of 268 GHz for beyond 5G application <i>Angelin Delight A, Binola K Jebalin. I.V, Ancy Michel, and D. Nirmal</i>	283-288
57	Rapid detection of Biomolecules by Quarapul cavity extended source vertical Dielectric Modulated TFET (QESV-DM-TFET) Biosensor <i>Nelaturi Nagendra Reddy, Bitra Jayalakshmi, Goli Srinivasa Rao, Deepak Kumar Panda, Sarankumar Ramasamy and Mandem Nomitha Reddy</i>	289-293

58	Performance investigation of L-shaped extended source TFET based photosensor for near-infrared light sensing applications	294-297
	<i>Chinna Baji Shaik, Anil Kumar. Pathakamuri, Kadava R. N. Karthik, Gorla Siva Rama Krishna, Ashok Tammiseti, Chandan Kumar Pandey and Umakanta Nanda</i>	
59	Performance Analysis of Double-Gate Junctionless Tunnel FET with a Stepped Channel	298-302
	<i>Siva Ramakrishna Gorla, Anil Kumar. Pathakamuri, Kadava R. N. Karthik, Ashok.tammiseti, Chinna Baji shaik S, Chandan Kumar Pandey and Umakanta Nanda</i>	
60	Optimization of Doping Profile in Carbon Nanotube Field Effect Transistor	303-307
	<i>Shuvra Jyoti Bose, Sneha Singh and Rudra Sankar Dhar</i>	
61	Supercapacitor-Based power delivery system to enhance the discharge duration for EVs	308-313
	<i>Harleenpal Singh, Sobhit Saxena and Vikram Kumar</i>	
62	Double gate Tunnel FET with Core-Gate Engineering: An Effective Approach to Suppress Ambipolarity	314-317
	<i>Meenu Sharma, Vanshika Ghai, Sidhartha Dash and Guru Prasad Mishra</i>	
63	Simulation of Adaptive Wavelet Packets in Spatial Domain for Signal Demodulation in Optical Frequency Domain Reflectometry	318-322
	<i>Nandini Basumallick and Somnath Bandyopadhyay</i>	
64	Study on Optical Properties of Multiple Quantum Well-based InGaN/GaN Light Emitting Diode	323-326
	<i>Devika Jena, Ajit K.Sahu, Sanghamitra Das and Narayan Sahoo</i>	
65	Comparative Study of MEMS Microheaters using distinct designs and materials for PCR applications	327-332
	<i>Pallavi Patel, Vinod Belwanshi, Neela Chatteraj and Richa Mishra</i>	
66	Understanding and Enhancing Linearity in FinFET Biosensors for Biomolecule Detection	333-336
	<i>Prasant Kumar Swain, Debasish Nayak, Prakash Kumar Rout, and Sudhansu Mohan Biswal</i>	
67	Synthesis of Graphite-Based Conductive Paint for Flexible Paper Electrode for Voltammetric Detection of Lawsone in Cosmetic Product	337-342
	<i>Milan Dhara, Sanjoy Banerjee, Hemanta Naskar, Barnali Ghatak, SK. Babar Ali, Rajib Bandyopadhyay, Nityananda Das and Bipan Tudu</i>	
68	Design and study of the thermoelectric performance of mini cooler box using TEC	343-348

	<i>Shreya Adhvaryyu, Parimal Acharjee and Kalyan Kumar Mistry</i>	
69	Optimizing Triple Material Staggered Heterojunction Double Gate MOSFET (TM-SH-DGMOS) Through Advanced Gate Engineering <i>Prasant Kumar Swain, Kishore Chandra Singh, Biswajit Baral, and Sudhansu Mohan Biswal</i>	349-352
70	Quasi Vertical FinFET with Step Graded Doping for Obtaining 0.037 mΩ.cm² ON Resistance <i>Ancy Michel, Binola K Jebalin. I.V, Navin M George, Angelin Delighta A and D. Nirmal</i>	353-357
71	Performance Investigation on Gate Stack Dual Material Double Gate MOSFET based Biosensor <i>Satish K. Das, Sudhansu M. Biswal, LalatIndu Giri and Umakanta Nanda</i>	358-361
72	Enhanced Sensitivity in InAs Based Gate Stack TFET Biosensors: An In-Depth Investigation <i>Kishore Ch Singh, Prasanta Ku Khuntia, Satish Ku Das, Sudhansu M Biswal, Biswajit Baral and Sarita Misra</i>	362-365
73	Design And Comparison of 4x4 Bit Multipliers Utilizing CMOS 45nm And FinFET Technology <i>Chirag Jain, Mohit Kumar Goel, Lipika Gupta and Kulbhushan Sharma</i>	366-370
74	Linearity Characteristics of Gate-Stack DG-MOSFETs: A Study with Diverse Biomolecule Configurations <i>Pritipadma Mohanty, Kishore Singh, Sanjit Swain and Sudhansu Biswal</i>	371-374
75	Analog/RF performance and reliability investigation of nanowire junctionless MOSFET with interface traps <i>Sarita Misra, Sudhansu Biswal, Satish Das, Kishore Singh and Kaliprasanna Swain</i>	375-378
76	Polarization Engineering of the EBL to Produce Efficient AlGaIn-based UV-C LED <i>Balkrishna Choubey and Kankat Ghosh</i>	379-382
77	High Temperature Performance Analysis of AlGaIn/GaN HEMT <i>Sanghamitra Das, Devika Jena, Eleena Mohapatra, Taraprasanna Dash and Aruna Tripathy</i>	383-386

78	High-endurance contention-aware power optimized hybrid memory using clock gating memory	387-392
	<i>Narayana Murty N, Harjit Singh and Sukhmani K. Thethi</i>	
79	Improvement in Toxic CO Detection Capabilities via Incorporating Pt Dopant into ZnO Nanotube based Gas Sensor Devices: An Atomistic Modeling	393-398
	<i>Indranil Maity, Siddhartha Bhattacharya and Aheli Majumdar</i>	
80	A Comprehensive Sensitivity Analysis of Adenine Nucleobase on Pristine and Platinum-Decorated ZnO Nanosheets: An Interaction Dynamics	399-404
	<i>Indranil Maity, Snehadri Bhaumik and Subhradeep Hazra</i>	
81	Customized Design and Optimization of New Materials in Silvaco TCAD Tool by Understanding Inherent Material Defining Processes and Useful Simulation Methods: An Extensive Study	405-410
	<i>Indranil Maity and Arijit Mondal</i>	
82	Studies on navigational satellite visibility and signal strength of different GNSS sensor	411-414
	<i>Debipriya Dutta, Somnath Mahato, Pritul Kumar Roy, Jeet Gorain, Soumya Kundu and Divyesh Deshpande</i>	
83	A transient enhanced capacitor less 380mA LDO with 1.2μA quiescent current	415-419
	<i>Sayantana Samanta, Joydeep De, Srijit Mishra, Soumik Bandyopadhyay and Swarnil Roy</i>	
84	A Low Leakage Variations and High Stability 9T SRAM Cells	420-425
	<i>Guguloth Anjaneyulu, M Durga Prakash, Mukku Pavan Kumar and Shams UI Haq</i>	
85	Design and Investigation of Ge Source Hetero-Dielectric L-shaped TFET for Low Power Applications	426-431
	<i>Mukesh Kumar, Aditya chotali, Seema Singh, Jemma Jessy Kerketta, Chhavi Rani, Vashnavi Nenavath, Santashraya Prasad and Aminul Islam</i>	
86	Analysis of Interface Trap Position Variation in Tunnel FETs	432-435
	<i>Anirudh Koteswar, Deepjyoti Deb, Shanidul Hoque and Rupam Goswami</i>	
87	Attention-COVIDNet: An Enhanced COVID-19 Classification Framework using Attention Mechanism	436-441

	<i>Senthil Pandi S, Thomas Leonid, Suguna Devi R and Sathish Kumar Kannaiah</i>	
88	Effective Webshell Detection in IoT Networks employing TF-IDF, Word2Vec and SVM	442-447
	<i>Senthil Pandi S, Masoodhu Banu N M, Suguna Devi R and Sathish Kumar Kannaiah</i>	
89	Assessment of FinFET Performance and Its Biosensing Applications: A Review	448-453
	<i>R.Linie Sharon and A.Shirly Edward</i>	
90	Enhancing Safety in Automotive Systems: A Comprehensive Analysis of 77 GHz Radar Performance for Pedestrian and Vehicle Detection	454-459
	<i>A Usha Rani, Aggala NagaJyothi and Sarika Nair</i>	
91	Fabrication, Characterization and SPICE Simulation of Dropcasted Egg Albumin Memristors	460-463
	<i>Hirakjyoti Choudhury, Rupam Goswami and Raja Vipul Gautam</i>	
92	Performance Evaluation of Double Gate Junctionless Accumulation Mode Stacked Gate MOSFET.	464-467
	<i>Pradipta Jena, Srikrishna Bardhan, Sarita Misra, Sudhansu Kumar Pati, Biswajit Baral, and Sudhansu Mohan Biswal</i>	
93	Analog and High Frequency Analysis of Dielectric Pocket Engineered (DPE) 4H-SiC Based Dual Metal(DM), Gate-Stack (GS), Surrounding Gate, FET(DPE-4H-SiC-GSDM-SGFET) for GIDL Reduction	468-473
	<i>Neeraj, Shobha Sharma, Anubha Goel, Sonam Rewari, S S Deswal and R S Gupta</i>	
94	Junction-less Nanowire TFET with HfO₂ /SiO₂ stacked gate-oxide for highly sensitive biosensor	474-477
	<i>Mandalaneni Jaya, Rohit Lorenzo and Sudheer Prajapati</i>	
95	Effects of Gate Metal Engineering on Electrical Characteristics of SOI MOSFET	478-481
	<i>Sonam Khera, Neetu Gupta, Prashant Kumar, Lalit Rai, Neeraj Gupta and Rashmi Gupta</i>	
96	Predicting Tea Quality Based on Antioxidant and Polyphenol Content Using Ensemble Machine Learning Model	482-487
	<i>Pratyusha Chatterjee, Debajyoti Mitra, Tanima Bhowmik, Rosalin Nath, Kakoli Dutta, Arpan Deyasi</i>	

97	Generating Diverse Facial Expressions and Orientations from a Single Image Using Conditional Generative Adversarial Networks	488-493
	<i>Roshan Rateria and Tanima Bhowmik</i>	
98	Accuracy Enhancement in Apple Leaf Diseases Detection and Classification Using VGG16	494-499
	<i>Senthil Pandi S, Shanmugapriya S, Gethara Gowri C and Kumar P</i>	
99	Using Machine Learning to Predict Constant Obstructive Pneumonic Infection	500-505
	<i>Kumar P, Vijayaraj A, Senthil Pandi. S and Venkatesh Prabhu Balakrishnan</i>	
100	A Study on Si-Si(1-x)Gex Nanowire Solar Cells using Monte Carlo Simulation	506-511
	<i>Abir Jana, Sharmistha Shee Kanrar, Bhaskar Gupta and Subir Kumar Sarkar</i>	
101	Vivaldi Antenna with Reconfigurable Rectangular Slots	512-518
	<i>Harish Sharma, Neeraj Gupta, Ved Prakash and Sukomal Dey</i>	
102	Design of second order low pass filter using inverter-based CMOS operational transconductance amplifier (OTA) through gm/ID Methodology	519-524
	<i>Remya Jayachandran, Edet Bijoy Kumaradhas and Arun S</i>	
103	IoT-Driven Automated Hydroponic System for Climate-Independent Indoor Crop Cultivation	525-530
	<i>Joy Samadder, Subhadip Roy, Somnath Mapa, Sagar Gharami, Jadav Chandra Das and Amit Ghosh</i>	
104	Performance analysis of MoS2/MASnI3/WSe2 based solar cell with more than 31% efficiency	531-535
	<i>Tania Das, Ayan Das and Mihir Mahata</i>	
105	Exploring the Potential of AlGaN/GaN HEMT using TCAD Simulations for Next-Generation Biosensors	536-541
	<i>Yashwant Singh, Ashish Kumar, Neeraj Gupta and Nisha Charaya</i>	
106	Advancements in Operational Transconductance Amplifiers (OTAs) for the Design, Applications, and Performance Optimization Techniques with hardware implementation	542-547
	<i>Pramath V., Pavithra G., Swapnil S. Ninawe and T.C. Manjunath</i>	

107	Impact of Defects on the Electronic Properties of (8,3) and (7,5) Carbon Nanotube Heterojunction	548-552
	<i>Achsah Gladith N and Anandan P</i>	
108	Impact of the Process Parameter Variation on Threshold Voltage of Short Channel Junctionless MOSFET	553-556
	<i>Keka Biswas, Sumit Som, Papiya Debnath and Manash Chanda</i>	
109	Design of Power-Efficient Built-in Self-Repair for Interleaved Memory Systems	557-561
	<i>Sowvik Dey and Amiya Karmakar</i>	
110	Design of Humanoid Hand with Adaptive Gripping Patterns using Vision Sensor	562-566
	<i>Aishwarya Palit and Naiwrita Dey</i>	
111	A First-Principle Investigation of Sc-Doped MoS₂ for Hydrogen Gas Detection	567-572
	<i>Bibek Chettri, Bikash Sharma, Sanat Das, Pronita Chettri, Prasanna karki and Pema Rinzing Bhutia</i>	
112	A First-Principle Study to investigate Electrical and Optical Properties of Tin Oxide	573-577
	<i>Nandita Sharma, Bikash Sharma, Sanat Das, Pronita Chettri, Prasanna karki, Roshan Pradhan, Bibek Chettri and Ashok Rao</i>	
113	DFT Study of P-Doped WSe₂ Monolayer-Based VOC Sensor for Diagnosis of Lung Cancer	578-582
	<i>Prasanna karki, Bikash Sharma, Sanat Das, Pronita Chettri, Ashok Rao and Bibek Chettri</i>	
114	Implementation of High-K Gate Dielectric in Cylindrical SOI Schottky Barrier MOSFET for Enhanced ION/IOFF Ratio	583-586
	<i>Nitish uppal, Amit Saxena, Vandana Nath and R.S. Gupta</i>	
115	Design and performance analysis of low noise amplifiers: A review	587-592
	<i>Saggurthi Spandana, Sk Hasane Ahammad and K Srinivasa Rao</i>	
116	Mapping Stress/Strain in Nanoscale FinFETs: Implications for Device Design	593-597
	<i>Taraprasanna Dash, Jhansirani Jena, Devika Jena, K V Subbarao, Subhashree Choudhury and C K Maiti</i>	
117	Analysis of Stress and Strain Dynamics in Sub-7nm GAA Si- and SiGe-Channel Nanosheet FETs	598-602
	<i>Taraprasanna Dash, Eleena Mohapatra, Jhansirani Jena, Sanghamitra Das, Subhashree Choudhury and C K Maiti</i>	

118	Junctionless Accumulation Mode Dual Gate Ferroelectric FET (JAM-DG-FE-FET) for High Cut-off Frequency Applications	603-606
	<i>Sagar Gosai, Sonam Rewari, Deva Nand and M Ganesh</i>	
119	Field Effect Transistor Incorporating Negative Capacitance and Nanowire Structures for the Attenuation of Gate Leakage Phenomena	607-611
	<i>Aapurva Kaul, Sonam Rewari and Deva Nand</i>	
120	A Comparative Power & Delay Analysis of Full Adder Designs in 90nm CMOS and 32nm & 5nm CNFET Technologies.	612-617
	<i>Aniruddha Sen, Nitish Kumar Sah, Kousik Bhunia and Sumit Saha</i>	
121	New Locally-Active Memristor for Neuromorphic Application	618-622
	<i>Parnab Das, Santanu Mandal, Mousami Sanyal and Soumyadip Chowdhury</i>	
122	Silicon Membranes for Microbolometers: Simulation and Fabrication Using Frontend Bulk Micromachining	623-628
	<i>Nirupam Paul, Satish Bonam, Siva Rama Krishna Vanjari and Shiv Govind Singh</i>	
123	Spoonie: Self-Stabilizing Feeding Spoon For Tremored Hands	629-633
	<i>Susmita Das, Ankit Kar, Hritabrata Ghosh, Priyanshu Das and Aniruddha Mitra</i>	
124	Effect of AlGa_N Thickness Variation on the Analog Performance of a Normally-off AlGa_N/Ga_N based Double Gate MOS-HEMT Device	634-638
	<i>Souptik Mallick, Souryob Ghosh, Chirayush Chakraborty and Atanu Kundu</i>	
125	A μW Power CMOS Window Detector Circuit with Adjustable Thresholds for Low-Power Applications	639-643
	<i>Uday Sannigrahi, Arkaprava Dash, Soham Banerjee, Koyel Mukherjee and Soumya Pandit</i>	
126	Analyzing the Analog performance of a Novel Normally OFF Double Gate MOS-HEMT due to Gate Length Variation	644-648
	<i>Sudipta Talukder, Aditya Shaw, Chirayush Chakraborty and Atanu Kundu</i>	
127	Enhancing Ultrasonic-Based Distance Measurement Accuracy Through Error Correction Mechanism	649-654
	<i>Abhijit Paul, Arjun Mitra, Prachi Bansal, Mudit Saraf, Bikash Debnat and Jadav Chandra Das</i>	
128	Performance Optimization of Thin Film Micro-Patterned Piezoresistive Low Pressure Sensor	655-660
	<i>Sekhar Rana, Santanu Maity, Rathindra Nath Biswas and Mrinal Kanti Naskar</i>	

129	A Fully-Customized RTL to GDS Design and Verification of Low-Power Cache Memory	661-666
	<i>Eleena Mohapatra, Sudeep Kumar Shetty, Sujatha Hiremath, Sanghamitra Das, Devika Jena and Taraprasanna Dash</i>	
130	Novel Modular Adder Using Thermometer Coding and One-Hot Coding for Residue Number Systems Applications	667-672
	<i>Kancharla Vijaya Vardhan, Musala Sarada and Talasila Jahnvi</i>	
131	Design of VTFET based biosensor utilizing Ambipolar Current in detection mechanism	673-677
	<i>Parmita Roy, Abhigyan Hazarika and Gaurav Trivedi</i>	
132	Investigating the device and circuit level performance of nanoscale double gate junctionless transistors	678-682
	<i>Sandeep Kumar, Kulbhushan Sharma and Chusen Duari</i>	
133	Effect of Hole Transport Layer on Tin based Perovskite Solar Cells	683-686
	<i>Somnath Dasgupta, Mihir Kumar Mahata, T. Das, A. Sarkar, Gufran Ahmad and Syed Sadique Anwer Askari</i>	
134	Photovoltaic Performance Analysis of Nanostructured GaAs 1-x Bi x Solar Cell for Mole Fraction 'x'=0.01	687-691
	<i>Debamita Roy, Dip Prakash Samajdar and Abhijit Biswas</i>	
135	Theoretical Investigation of CsSn1-xGexI3 perovskite solar cells using Graded Bandgap Profiles	692-695
	<i>Arya Narayanan, Babban Ravidas and Dip Prakash Samajdar</i>	
136	Investigation of the Recombination Processes in FA0.75Cs0.25SnI3~based Perovskite Solar Cell: A Theoretical Framework via SCAPS-1D	696-700
	<i>Babban Kumar Ravidas, Mukesh Kumar Roy and Dip Prakash Samajdar</i>	
137	On the Potential of HEMT for Millimeter-Wave Applications and Integrated Circuits for 5G Transceivers: A Review	701-705
	<i>Kamal Bhatia, Yogesh Kumar Verma, S. K. Hima Bindhu and Yashika Bhatia</i>	
138	An ab initio Study of Sub-5nm Monolayer Double-Gate Arsenene/Antemonene Junctionless Field Effect Transistors	706-709
	<i>Alokesh Mondal, Anup Dey, Biswajit Maity and Manash Chanda</i>	

139	Exploring the potentials of a lateral p-n junction by using novel approach	710-713
	<i>Sriyanka Behera, Gananath Dash and Satya R. Pattanaik</i>	
140	Comparative Performance Analysis of Dual FinFET and Gate-All-Around Triple Nanosheet FET for 5 nm Node	714-719
	<i>Ram Krishna Dewangan, Vinay Kumar Singh and Mohammad Rafique Kha</i>	
141	Analysis of Membrane Yield in Insulated Air-Patched Capacitive Transducers for High-Frequency Applications	720-725
	<i>Bijit Kumar Nath, Reshmi Maity and Niladri Pratap Maity</i>	
142	Parametric Studies of a Clamped-to-Clamped Resonant Beam Microelectromechanical System Based Accelerometer	726-732
	<i>Mrinmoy Singha, Reshmi Maity and Niladri Pratap Maity</i>	
143	Predictive modeling of Nanoscale Junctionless FinFET using XGBoost	733-736
	<i>Rachita Ghoshhajra, Kalyan Biswas, Mahamuda Sultana and Angsuman Sarkar</i>	
144	Sensitivity Investigation of Gate Stack Junctionless GaAs FinFET based NH₃ Gas Sensor	737-741
	<i>Divya Babbar, Neha Garg and Sneha Kabra</i>	
145	Enhanced Crop Yield Prediction by Machine Learning Techniques	742-747
	<i>Papiya Das, Abhranil Pal, Rakteem Mullick, Sayak Singha and Subhprapatim Nath</i>	
146	Digital Predistortion Behavioral Modeling of Power Amplifiers: A Neural Network-Based Approach to Nonlinearity Compensation	748-753
	<i>Hemant Kumari, Amartya Paul and Shubhankar Majumdar</i>	
147	Study of Electrical Characteristics and Charge Storage Behaviour of Gold Embedded Floating Gate MOS Structure.	754-758
	<i>Amrita Banerjee, Gargi Chakraborty and Sunipa Roy</i>	
148	Optimizing Si-Based DG-JL-TFET Performance through Tunable Work function Engineering	759-764
	<i>Tamilarasi R and Karthik S</i>	
149	Design and Implementation of Low Power Circuits based on 5nm Double Gate MOSFET Technology using Different Materials	765-770

	<i>Shrabanti Kundu and Jyotsna Kumar. Mandal</i>	
150	Comparative Analysis of Electrical Parameters for High Electron Mobility Transistors	771-774
	<i>Yogesh Kumar Verma and Kamal Bhatia</i>	
151	Kernel Based Fuzzy Simulation Model for Early Detection of Cancer to Avoid Metastasis	775-778
	<i>Soumen Santra, Dipankar Majumdar, Surajit Mandal and Arpan Deyasi</i>	
152	Design and implementation of CML frequency divider circuit using 90nm Technology	779-784
	<i>B.Khaleelu Rehman, Ramgiri Sreeja, K Venkata Siva Reddy, P.Anuradha, Mohammed Abdul Nasar and Mudasar Basha</i>	

Chaotic Image Encryption Scheme Implemented in FPGA for Security Enhance

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90
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Abstract

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- I. Introduction
- II. Proposed Method
- III. Result Analysis
- IV. Conclusion

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Abstract:

The internet has always faced significant security challenges when it comes to transferring information. Throughout and following the recent outbreak, it has become evident that as digital transactions surge, so do incidents of hacking and breaches. This highlights the growing need for secure transaction methods. In response, this paper introduces a novel cryptographic approach for image encryption and decryption, utilizing chaotic algorithms. To ensure the robustness of the encryption, we perform a series of rigorous performance evaluations, including Histogram, Entropy, NPCR, UACI Analyses. This study showcases the implementation of a one-dimensional reduce Henon chaotic map on an FPGA board, enhancing both the encryption and integrity of images.

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I. Introduction

Chaotic events have a broad spectrum of engineering and scientific uses, such as secure data transmission, nonlinear control, and image encryption [1]. Researchers largely agree that chaos-based systems can be built using FPGA boards, discrete electronic components [2]. The advent of field-programmable gate arrays (FPGAs) has accelerated the process of prototyping hardware, making it more accessible [3]. Many scholars are now employing FPGAs to quickly prototype new hardware for chaotic systems, memristors, and various non-clonable type of functions [4].

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Authors

[Pradipta Sarkar](#)

Department of ECE, Dr. B. C. Roy Engineering College, Durgapur, India

[Anup Kumar Das](#)

Department of ECE, Dr. B. C. Roy Engineering College, Durgapur, India

[Aloke Saha](#)

Department of ECE, Dr. B. C. Roy Engineering College, Durgapur, India

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