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Automated Design of CMOS-DACML Circuit

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Abstract

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This paper presents a new method for designing a differential amplifier using CMOS technology, incorporating a current mirror load (CMOS-DACML). To tackle the intricate optimization challenges presented by this nonlinear and multidimensional problem, the study utilizes a combined optimization strategy called fitness-based adaptive differential evolution with particle swarm optimization (ADEPSO). Through this hybrid approach, the design achieves substantial enhancements across critical performance metrics. Specifically, it achieves a notable reduction in power dissipation, lowering it to 520.60 μW. Moreover, the amplifier demonstrates a higher gain of 44.70 dB, significantly reduced output capacitance of 4.20 pF, and an enhanced cutoff frequency reaching 103.60 kHz. These outcomes highlight the effectiveness of ADEPSO in tackling the intricate challenges associated with differential amplifier design, especially in the context of CMOS-DACML. By optimizing these parameters simultaneously, the approach not only improves performance metrics but also underscores its potential for future applications in integrated circuit design and optimization.

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***Abstract*—This paper presents a new method for designing a differential amplifier using CMOS technology, incorporating a current mirror load (CMOS-DACML). To tackle the intricate optimization challenges presented by this nonlinear and multidimensional problem, the study utilizes a combined optimization strategy called fitness-based adaptive differential evolution with particle swarm optimization (ADEPSO). Through this hybrid approach, the design achieves substantial enhancements across critical performance metrics. Specifically, it achieves a notable reduction in power dissipation, lowering it to 520.60 μW. Moreover, the amplifier demonstrates a higher gain of 44.70 dB, significantly reduced output capacitance of 4.20 pF, and an enhanced cutoff frequency reaching 103.60 kHz. These outcomes highlight the effectiveness of ADEPSO in tackling the intricate challenges associated with differential amplifier design, especially in the context of CMOS-DACML. By optimizing these parameters simultaneously, the approach not only improves performance metrics but also underscores its potential for future applications in integrated circuit design and optimization.**

***Index Terms*—analog circuits, circuit sizing, current mirror, differential amplifier, optimization**

I. Introduction

Circuit design optimization poses numerous challenges due to the diverse constraints, variables, and objective functions involved. Researchers have extensively explored various methodologies to automate analog circuit design, each with its advantages and limitations. One prominent approach is the equation-based method, where circuit sizing is managed through mathematical formulations [1]. This method offers rapid automation but often sacrifices accuracy in favor of computational efficiency. In contrast, optimization-based approaches prioritize refining circuit performance across multiple constraints, involving intricate design trade-offs. This typically necessitates iterative processes to fine-tune transistor sizes but achieves greater accuracy throughout the integrated circuit (IC) design cycle.

Artificial intelligence has also found application in modeling and optimizing analog and mixed-signal circuits, as discussed in [2].For example, [3] investigates the design and modeling of an active-loaded differential amplifier employing Double-Gate MOSFETs, demonstrating advancements in transistor technology. Sustainable engineering principles applied to MOSFET differential amplifiers are explored in [4], emphasizing performance enhancement through optimization strategies. Furthermore, Modern transistor technologies, such as FinFETs, are pivotal in achieving higher performance metrics, as evidenced by the analysis of a 20 nm gate length operational amplifier in [5].

Analytical approaches for minimizing losses in differential amplifiers using Double-Gate MOSFET technology are addressed in [6], underscoring the importance of advanced transistor models in circuit optimization. Efficient optimization methods play a crucial role in synthesizing analog circuits. For instance, a batch constrained Bayesian optimization method is introduced in [7]. Interactive evolutionary approaches are employed in optimizing low-noise amplifiers [8], showcasing diverse algorithmic applications in analog IC design. Swarm intelligence and evolutionary algorithms are advancing rapidly, as highlighted in recent studies [9], [10] that investigate the design and optimization of analog integrated circuits. A recent study highlight the application of machine learning techniques in automated sizing and fault diagnosis of complex analog circuits [11], reflecting ongoing innovations in circuit optimization methodologies.

This paper primarily aims to present a new metaheuristic method called ADEPSO, designed for optimizing the design of CMOS differential amplifier circuits with current mirror load (CMOS-DACML). This approach aims to enhance amplifier gain while minimizing the CMOS area. ADEPSO combines the PSO with the differential evolution (DE) algorithm, employing a fitness adaptation strategy tailored for solving global optimization tasks. Compared to the genetic algorithm, ADEPSO requires fewer basic mathematical operations, streamlining the optimization process. The design problem is formulated using an equation incorporating design and input variables as a cost function. Simulation results validated using the SPICE simulator demonstrate that the proposed ADEPSO-based amplifier achieves superior performance metrics, includ-