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New Scalable 32 nm CMOS Radix-3 Priority Encoder

Aloke Saha[1], Priyanka Saha[1] and Dipankar Pal[2]

[1]Department of ECE, Dr. B. C. Roy Engineering College, Durgapur, India; [2]Department of EEE & EI, BITS-Pilani, K. K. Birla Goa-Campus, Sancoale, India

ABSTRACT

The present endeavour presents a novel circuit topology for low-power-delay-product (PDP), scalable unary-to-ternary priority encoder (U-TPE) using conventional enhancement-MOS-devices. The theoretical aspect of a 3:1 U-TPE is explored first and extended to propose a 9:2 and a 27:3 U-TPE using scalability. The front-end circuit is designed based on the BSIM4 model parameters and 32 nm conventional CMOS technology at 0.9 V supply rail at 27°C temperature. The designed circuit is validated through extensive T-Spice simulations by applying custom trit-patterns through Piece-Wise-Linear (PWL) input source. The voltage level of 0 V (ground), 0.45 V (supply/2), and 0.9 V (supply) represent the unbalanced ternary digits (trits) "0", "1", and "2", respectively. The physical design of the proposed U-TPE is completed and presented based on 32 nm single-poly double-metal (SPDM) CMOS process technology. The layout is verified through the design rule check (DRC) first and layout-vs-schematic (LVS) next. The post layout simulation with extracted parasitic is performed at 27°C temperature and 0.9 V supply on 1fF load, and the result is tabulated. A benchmarking exercise with other candidate designs (both ternary and binary) proves the efficiency of the proposed work. A 3-trit ternary comparator designed with 9:2-U-TPE, and compared with a recent work from open literature exhibits its application potential. Finally, the robustness of the proposed U-TPE is measured by applying possible process voltage temperature (PVT) variation by considering ±10% supply variation from nominal with fast, typical and slow transistor over the temperature range from −40°C to +85°C. The worst-case performance with 1, 5 and 10fF load is recorded.

KEYWORDS

Number system; Priority encoding; PVT-analysis; Ternary multiplexing; T-Spice simulation

1. INTRODUCTION

Priority encoder (PE) is one of the prime building blocks in real-time big-data processing systems and finds wide applications in the area of industrial automation, real-time health-care/environmental monitoring, robotics, multi-match detection in content addressable memory (CAM) [1–13], among others. Globally accepted 2-valued binary system for digital design is currently reaching saturation and suffers from interconnect overhead, signal integrity with fan-in/out issue, circuit reliability due to hot-spot, uncontrollable clock-skew [14], *etc*., mainly in high-resolution sophisticated smart system development, which is currently in demand. To address this multi-valued ternary (base-3) system attracted concurrent researches in recent past [15,16] and is trendy in the present-scenario [17–24] because it shows higher efficiency by utilizing lesser number of component module yet carrying relatively more information for identical data processing as compared to its binary based counterpart [14,20]. Moreover, the base-3 (ternary) radix system is the closest to the natural base-e (≈ 2.72) and includes the least post-conversion digital error with respect to other MVL (multi valued logic) systems [17]. As a consequence, the ternary priority encoder (TPE) [25,26] appears to be only a logical choice for base-3 (ternary) data processing. Yet very few designs are found in open literature, and this aspect specifically has been the motivation behind this work.

Therefore, we present a new scalable unary-to-ternary priority encoder (U-TPE) with standard process enhancement mode MOS transistors. The concept is first applied to propose a 3:1 U-TPE and is next exploited to design a 9:2 U-TPE by applying scalability. The 9:2 U-TPE is further scaled-up to present a 27:3 U-TPE as the final implementation of the proposed concept and also as the testimony of the scalability of the design. The front-end design and optimization of the proposed circuit are completed on 32 nm conventional CMOS technology with BSIM4 model transistor parameters at 0.9 V supply rail and at 27°C temperature using the schematic editor (S-Edit) of Tanner EDA. The "ground", "Supply/2", and "Supply" are selected to represent the ternary digits "0", "1", and "2" respectively. The T-Spice transient simulations with all possible test patterns using piece-wise linear (PWL) input source validated the circuit operation of the proposed priority encoder. The physical design/layout of the proposed Encoder is made with 32 nm SPDM CMOS