Computers and Electrical Engineering 123 (2025) 110041

Contents lists available at ScienceDirect

Computers and Electrical Engineering

journal homepage: www.elsevier.com/locate/compeleceng

Enhancing predictive accuracy using machine learning for network-on-chip performance modeling

Ramapati Patra [a,*], Prasenjit Maji [a,b], Yogesh Raj [a], Hemanta Kumar Mondal [a]

[a] NIT Durgapur–ECE, M.G. Road, Durgapur, 713209, WB, India
[b] Dr. B.C.Roy Engg. College Durgapur–CSD, Jemua Road, Durgapur, 713206, WB, India

ARTICLE INFO

Keywords:
Cycle-accurate simulator
Performance enhancement
Machine learning
Network-on-chip (NoC)
Regression models

ABSTRACT

Network-on-Chip (NoC) is a promising, scalable interconnect solution of System-on-Chip (SoC) designs for high-performance computing platforms. The critical metrics, such as latency, throughput, and the number of packets received, directly impact the overall performance of NoCs. However, a cycle-accurate simulator takes considerable execution time with system size. This work proposes a machine learning approach with various regression models to predict critical metrics for network-on-chip-based architectures. The proposed work explores Polynomial regression (PR), Linear regression (LR), and Decision tree regression (DTR) models to predict linear and non-linear performance metrics. The obtained results are compared with the dataset generated from a cycle-accurate simulator. The experimental results showed an accuracy of 99% for linear and up to 98% for non-linear outputs with a maximum speed of around 3600x compared to a cycle-accurate simulator. Testing our model with SPLASH-2 and PARSEC real and synthetic benchmarks outperformed the existing works due to the convincing nature of real traffic.

1. Introduction

Network-on-Chip (NoC) architectures have become the most efficient fabric for connecting multiple Intellectual Property (IP) and multi-core systems. The emerging NoC interconnection infrastructure may be utilized for various heavy-workload applications, such as image and video processing and communication [1]. A high-performance NoC would be a better solution to boost the overall system performance. Network-on-Chip communication infrastructure offers potential and scalable solutions for complex applications. The complexity increases over time to achieve the desired performance in terms of power, and cost [2]. Therefore, there is a great need for efficient on-chip interconnection architecture for high-performance computing platforms.

The NoC is one of the suitable candidates for high-performance computing platforms. Researchers first developed and tested an application model using NoC simulators to simulate various architecture models. NoC simulators such as Noxim [3], PatNoxim [4], Booksim2.0 [5], SICOSYS [6], and Nirgam3 [7] are developed to explore the NoC-based segments and sub-design space before the actual hardware implementation. The Noxim simulator is one of the best cycle-accurate simulators for NoC architectures. The SystemC-based Noxim Runtime Engine (NRE) is explored to implement the different NoC architecture models and elements [8]. The NRE supports various topologies, packet and buffer sizes, traffic distributions, routing algorithms, and packet injection rates (PIR) to generate latency, throughput, and energy. For complex NoC architecture, the existing simulator is indifferent over the time frame. As a consequence, a fast approach to inspecting NoC designs is necessary.

* Correspondence to: Department of Electronics and Communication Engineering, National Institute of Technology (NIT) Durgapur, Mahatma Gandhi Avenue, Durgapur 713209, West Bengal, India.
E-mail address: ramanaatpatrra@gmail.com (R. Patra).

https://doi.org/10.1016/j.compeleceng.2024.110041
Received 7 February 2024; Received in revised form 31 March 2024; Accepted 24 December 2024
Available online 7 January 2025