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Machine learning-driven performance assessment of network-on-chip architectures

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Abstract

System-on-chip designs for high-performance computing systems widely use network-on-chip (NoC) technology. The critical metrics such as latency, throughput, and total energy directly impact the performance of NoCs. However, a cycle-accurate simulator takes considerable execution time for different values of packet injection rate. This paper proposes a machine learning approach with various regression models to predict the essential NoC performance metrics. The work explores regression models, including decision trees, K-nearest neighbors, random forest, polynomial regression, and support vector regression, alongside baseline linear regression for 2D and 3D NoC-based architectures. Experiment results demonstrate high accuracy, ranging from 96.72 to 99.96% for 2D and up to 99.99% for 3D NoC-based architectures. Root-mean-squared error values vary from 0.2792 to 0.03143 for 2D NoC and 0.1857 to 0.0063 for 3D NoC architecture. The proposed framework achieves impressive speedup, reaching up to 4678.8X and 46152.8X for system sizes 8×8×4 and 10×10×20, respectively.

Keywords Machine learning approach · High-performance computing · Performance assessment · 2D and 3D network-on-chip · Regression models

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