



Proceedings of
5th International Conference
on
2023 Devices for Integrated Circuit (DevIC)

7-8 April, 2023, Kalyani, Nadia, India

Organized by

IEEE KGEC Student Branch Chapter

In association with

Department of ECE, Kalyani Government Engineering College

Edited by

Dr. Angsuman Sarkar
Dr. Sandip Nandi

Kalyani Government Engineering College

2023 Devices for Integrated Circuit (DevIC)

Copyright and Reprint Permission: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For reprint or republication permission, email to IEEE Copyrights Manager at pubs-permissions@ieee.org. All rights reserved. Copyright ©2023 by IEEE.

Part Number: CFP23K13-ART

ISBN: 979-8-3503-4726-5

Table of Contents

	Page No.
Message from the General Chair	xi
Message from the Editors	xii
1. Enhancing the Performance of Electrostatically Doped Double POLO PERC Solar Cell through Metal Silicides <i>Savita Kashyap, Rahul Pandey, Jaya Madan and Rajnish Sharma</i>	1-4
2. Design of Low power and High-Performance Decoder Using Carbon Nanotube Field Effect Transistor (CNTFET) <i>Prashant Kumar, Neeraj Gupta, Lalit Rai, Rashmi Gupta</i>	5-8
3. 1-bit Magnitude Comparator based on Reversible Logic using QCA Technology <i>Vaishali Dhare and Divy Modi</i>	9-12
4. Gate Engineered IGBT with Improved Device Performance <i>Satish Kumar Sahu, Saji. T. Chacko, Onika Parmar and Amit Singh Rajput</i>	13-16
5. Performance Analysis of Low Power Multiplexer for Communication System <i>Lalit Rai, Neeraj Gupta, Prashant Kumar, Rashmi Gupta</i>	17-21
6. Input Variable Bypass or IVB Technique for Logic Functions Simplification <i>Heranmoy Maity, Parna Kundu, Aritra Bhowmik and Arijit Kr Barik</i>	22-25
7. Implementation of the Quantum BCD-to-Excess-3 Code Converter using New Quantum Reversible Circuit Block <i>Parna Kundu, Heranmoy Maity, Aritra Bhowmik and Biswajit Roy</i>	26-29
8. Comparative Analysis of EEPL and PPL Techniques in 18nm FinFET Technology <i>Gautam Rana, Kulbhushan Sharma, Anjali Sharma, Lipika Gupta and Ashish Sachdeva</i>	30-33
9. Design and Simulation of Cascode Current reuse low power Operational transconductance amplifier <i>Ravi Kumar, Kulbhushan Sharma, Ashish Sachdeva and Lipika Gupta</i>	34-37
10. Optimizing Photovoltaic Performance of MASnPbI₃ Perovskite Solar Cells through Layer Thickness Variations <i>Savita Rawat, Nikhil Shrivastav, Rahul Pandey and Jaya Madan</i>	38-41
11. Slotted Waveguide Antenna for Microwave Remote Sensing Applications	42-47

5th International Conference on “2023 Devices for Integrated Circuit (DevIC)”

Mandar Chakrabarti, Malay Ganguly and Abir Chattopadhyay

12. **One Dimensional Chaotic map Implementation in FPGA board for Image Encryption** 48-51
Pradipta Sarkar, Anup Das and Alope Saha
13. **Impact of Doping Variation on the Performance of Sb₂S₃ based Solar Cell using Device Simulations** 52-55
Vishal Yadav, Savita Kashyap, Rahul Pandey and Jaya Madan
14. **Towards Energy-Efficient Cost-Effective Toffoli Gate Design using Quantum Cellular Automata** 56-60
Debasmita Manna, Chiradeep Mukherjee, Ananya Banerjee, Manali Dhar, Saradindu Panda and Bansibadan Maji
15. **Analysis of FDSOI-Negative Capacitance MOSFET with Respect to Different Oxide Thickness and Temperatures** 61-66
Vydhya Pradeep Kumar and Deepak Kumar Panda
16. **Study on the impact of CuI as Hole Transport Layer (HTL) for CZTS-based Solar Cell** 67-70
Pratap Kumar Dakua, Dr Deepak Kumar Panda, A Laidouci and Sradhanjali sahu
17. **Threshold Voltage Analysis of E-mode Recessed p-GaN Gate HEMT-A Simulation Based Study** 71-76
Hindol Bhattacharjee, Anup Dey and Avishek Saha
18. **Design and Modeling of a Label-free JLTFET Based Biosensor for Enhanced Sensitivity** 77-81
Pratikhya Raut, Umakanta Nanda and Deepak Kumar Panda
19. **A Deep Learning Aided Intelligent Framework for Condition Monitoring of Electrical Machinery** 82-86
Biswarup Ganguly, Radha Kumari Ray, Arunava Chatterjee and Subho Paul
20. **Novel 32nm CMOS Ternary 3's Complement Generator** 87-91
Sudeshna Dutta, Snigdha Dutta, Osman Hossain Siddique, Rimpa Dey And Alope Saha
21. **Augmenting CIGS Solar Cell Efficiency through Optimization of Layer Thickness and Front Electrode Transparency** 92-95
Nikhil Shrivastav, Rahul Pandey and Jaya Madan
22. **Gate Modulated Graphene Channel TFET with Enhanced Switching Current Ratio** 96-99
Abhijit Panda, Sidhartha Dash and Guru Prasad Mishra
23. **Dielectric-Pocket based Multi-channel Nanowire Field Effect Transistor for High-speed Operations** 100-103
Ushodaya Ayyala Soma Yajula, Girija Sahoo and G. P. Mishra
24. **Improvement of Electron Transport in Pseudomorphic In_{0.52}Al_{0.48}As/In_yGa_{1-y}As Double Quantum Well Structure** 104-107

5th International Conference on “2023 Devices for Integrated Circuit (DevIC)”

*Ram Chandra Swain, Ajit K. Sahu, Narayan Sahoo, Madhusudan Mishra and
Trinath Sahu*

25. **Low Lead All-Inorganic Hybrid Perovskite: A Study of Interface Defects using SCAPS-1D** 108-112
Navdeep kaur, Jaya Madan and Rahul Pandey
26. **Sensitivity Analysis of MEMS-based Piezoresistive Pressure Sensor Implementing Ritz Method** 113-118
Kakali Das and Himadri Dutta
27. **Device Performance Analysis for Different Gate Locations in AlGaIn/GaN HEMT by Silvaco Simulation** 119-123
Mihir Mahata, Soumyadip Chatterjee, Tania Das and Angsuman Sarkar
28. **Characterization and Thermal Steadiness of Trenched stepped gate SON MOSFET for future CMOS devices** 124-128
Sikha Mishra, Guru Mishra and Soumya Mohanty
29. **Truncated Corner and Slotted Wearable Textile Multiband Antenna for Wireless Applications** 129-133
Geetanjali Sharma, Neeru Kashyap, Shaminder Kaur and Poonam Jindal
30. **Implementation of Retiming Technique for Clock Period Optimization by Brute-Force Approach** 134-138
Vishwaraj Mahan and Manish Patel
31. **Performance Analysis of Double Gate MOSFET with High-k Dielectric** 139-143
Neeraj Gupta, Bal Krishan, Neelam Bedwal, Prashant Kumar, Ved Prakash
32. **Highly sensitive surface plasmon-based refractive index sensor in the optical communication band using ZnS-PVP layers** 144-147
Sambhavi Shukla, Sindura Patria, Ananya Singh and Pankaj Arora
33. **Effect of Electron Transport Layer on Tin based Perovskite Solar Cells** 148-151
Somnath Dasgupta, Syed Sadique Anwer Askari, Gufran Ahmad and Mihir Mahata
34. **Dibit-based Frequency encoded Fredkin gate** 152-157
Surajit Bosu and Baibaswata Bhattacharjee
35. **High Gain Farming and Data Analytics using IoT** 158-162
Manoj Singh Adhikari, Arunava Majumder, Ahmin Mukhthar Sheifudeen , Kamireddy Harshavardhan Reddy , Manoj Sidhwani and Yogesh Kumar Verma
36. **A Review on Emerging Tunnel FET Structures for High-speed and Low-power Circuit Applications** 163-167
Chandan Kumar Pandey, Diganta Das, Kadava R. N. Karthik, Tammisetti Ashok, Anil Pathakamuri and Siva Rama Krishna
37. **Investigation of 2D nanomaterials on Indium Phosphide-based plasmonic devices for sensing in the optical communication band** 168-172

5th International Conference on “2023 Devices for Integrated Circuit (DevIC)”

Sambhavi Shukla, Yash Tripathy, Kshitij Sanghi and Pankaj Arora

38. **Resonant Method for Determining the Dielectric Characteristics of A Mixture of Small Dispersed Bulk Materials at Ka-Band** 173-176
Alexander Kogut, Sergey Nosatiuk, Boutaina Benhmimou, Fatima Zahra Lamzouri, Rachid Ahl Laamara, Mohamed El Bakkali, Sandeep Kumar Arora, Praveen Kumar Malik and Rajesh Singh
39. **Performance Investigation of Inverted T-shaped Heterojunction FinFET along with Oxide Stacking** 177-181
Vishal Narula, Shekhar Verma, Suman Lata Tripathi, Balwinder Raj
40. **Single Layer Design of Dual Banyan Network Using Quantum-Dot Cellular Automata** 182-185
Jadav Chandra Das, Bikash Debnath, Debashis De and Angsuman Sarkar
41. **A Different Approach for Traffic Management System for Emergency Vehicles During Heavy Traffic for Biomedical Applications** 186-189
Sehan Balajee Pilli, Katha Raja Indra Sena Reddy, Abhinav Jain, Sumit Yadav, V. Naga Babu, Yogesh Kumar Verma
42. **Global horizontal irradiance and wind speed prediction using ANN : Comprehensive Study** 190-193
Pooja Malik, Praveen Kumar Malik, Rajesh Singh and Anita Gehlot
43. **Technical Intercession of Artificial Intelligence in Solving Online Dispute Resolution** 194-198
Samta Kathuria, Krishna Rastogi, Rajesh Bahuguna, Anita Gehlot, Praveen Malik and Prafful Negi
44. **Design of a Reliable Copyright Management System Based on Blockchain** 199-202
Samta Kathuria, Radhika Nautiyal, Radhey Shyam Jha, Anita Gehlot, Anil Kumar and Praveen Malik
45. **Cyber Physical System Role in Stock Market** 203-206
Samta Kathuria, Aadidevam Dhyani, Deepa Bisht, Anita Gehlot, Radhika Nautiyal and Sushabhan Choudhury
46. **Artificial Intelligence and Internet of Things Based Technological Advancement in Domain of Horticulture 4.0** 207-211
Samta Kathuria, Reemashree Das, Siddharth Shanker Bhatt, Rajesh Singh, Gunjan Chhabra and Praveen Malik
47. **Digitalization Transformation: Essence of Virtual Reality Indulging in the Mental Health of People** 212-216
Shweta Pandey, Navneet Shankar Pandey, Poonam Rawat, Rajesh Singh and Hardeep Kaur
48. **Enabling Technologies for Wildlife Conservation** 217-220
Shweta Pandey, Aarju Jangra, Rajesh Bahuguna, Rajesh Singh, Gunjan Chhabra and Sushabhan Choudhury
49. **Significance of Emerging Technological Advancements in Transition of Green Economy** 221-224

5th International Conference on “2023 Devices for Integrated Circuit (DevIC)”

- Shweta Pandey, Reeta Rautela, Shravan Kumar, Namrata Prakash, Anil Kumar and Praveen Malik*
50. **Investigation of Quantum Ballistic Transport in Single Strand DNA with Silicon Carbide Nanotube : A High performance Embedded System** 225-228
Debarati Dey Roy, Anirban Ghosal, Abhilasha, Nikki Singh, Nivedita Sinha and Swarnali Saha
51. **Subsuming AI, IoT and Big Data in Smart Farm Practices** 229-232
Shweta Pandey, Anita Gehlot, Vaibhav Pandey, namrata kathuria, Praveen Kumar Malik and Gunjan Chhabra
52. **Role of Technology Under Advancement of Industrialisation in Intellectual Property Rights** 233-236
Shweta Pandey, Rahul Pandey, Rajesh Bahuguna, Poonam Rawat, Rajesh Singh and Aditi Bansal
53. **High Gain Multistage CMOS Amplifier Design at 45nm technology node** 237-242
Suman Tripathi, Balwinder Raj, Shekher Verma, Vishal Narula and Sobhit Saxena
54. **Design of Secure Reversible Select, Cross and Variation (RSCV) Architecture in Quantum Computing** 243-247
Arpita Kundu, Jadav Chandra Das, Debashis De, Bikash Debnath and Angsuman Sarkar
55. **The Ground Switcher** 248-252
Usama Thakur
56. **AlGa_N/Ga_N based HEMT with AlN spacer and Nucleation layer for high power application** 253-256
Jadhav Swati Dhondiram and Aboo Bakar Khan
57. **IoT Based Monitoring of Environment in a Smart Hydroponic System** 257-260
M.K. Shukla, Archana Kanwar, Soumyadeep Raul, Agili Vishnu Sai and Bhupinder Verma
58. **Phase Transition Material modulated Hyper-FET for Digital Applications** 261-265
Ritika Sorot, Anubha Goel and Sonam Rewari
59. **Minimally Coupled E-Shaped Dual-band Antenna for Wireless Applications** 266-271
Sourav Bhattacharyya, Aritra Bhowmik and Karunamoy Chatterjee
60. **Intersubband effects on electron mobility in GaAs/ In_xGa_{1-x}As Quantum well FET with asymmetric doping profiles** 272-276
Sangita Rani Panda, Manoranjan Pradhan, Trinath Sahu and Ajit Kumar Panda
61. **An Offset-Fed T-Shaped Two-Port MIMO Antenna for 38 GHz 5G Millimeter-Wave band Applications** 277-281
Parminder Kaur, Shivani Malhotra and Manish Sharma
62. **9T SRAM Cell for Computation-In-Memory Architectures: Proposal & Investigation** 282-286

5th International Conference on “2023 Devices for Integrated Circuit (DevIC)”

*Aman Kumar Gupta, Prashant Joshi, Shobhit Srivastava, Sourabh Panwar,
Rajendra Singh Shekhawat, Abhishek Kilak, Shivendra Yadav, Deepak Joshi
and Abhishek Acharya*

63. **Analysis of SiGe, InGaAs and GaN on 5nm MOSFET Modelling with Applications** 287-290
Raktim Chakraborty and Jyotsna Kumar Mandal
64. **A Temperature Compensated Beta-Multiplier Based Sub-1 V Voltage Reference Circuit for Low-Voltage Applications** 291-295
Soham Banerjee, Soumita Chatterjee, Koyel Mukherjee and Soumya Pandit
65. **Design a self-charging electric vehicle with multiple natural energy sources** 296-301
Ramchandra Sahani, Manas Daga, Ishak Jamatia, Pavan Kumar and Suman Lata Tripathi
66. **Adaptable Terahertz absorber using circular shaped Graphene Metamaterial for LO Technology** 302-306
Lavanya B, Sagadevan K, Elizabeth Caroline Britto, Gayathri S and Mohamed Nizar S
67. **An Exploration of Photovoltaic Performance of the Rb₂SnI₆ using DFT and SCAPS-1D** 307-311
Babban Kumar Ravidas, Abhijit Das, Mukesh Kumar Roy and Dip Prakash Samajdar
68. **Efficiency Enhancement GaAs Ultra-Thin Solar Cell Using Anti-Reflection Coating** 312-315
D V Prashant, Suneet Kumar Agnihotri and Dip Prakash Samajdar
69. **An on-demand charging schedule utilizing multiple mobile charging vehicles for WRSNs** 316-320
Sk Md Abidar Rahaman, Md Azharuddin
70. **IOT Based Precision Agri-Bot** 321-324
Manoj Singh Adhikari, Kumaran Muthu Ramalingam, Abhinav Anand, Gokul Prasath Venkatesan, Aravind Raj Ravi and Naman Thakur
71. **Mechanical and Electrical Performance of Stretchable Honeycomb Interconnect With Aspect Ratio Variation** 325-329
Ananya Bhattacharjee and Ratul Kumar Baruah
72. **Configurable 8T SRAM-based Computing In-Memory Architecture for Enabling Shift Operation and Multibit Dot-Product Engines** 330-334
Chakka Yeswanth, Shobhit Srivastava, Shashidhara M, Sourabh Panwar, Deepak Joshi and Abhishek Acharya
73. **Design of a Catenary Shaped Multiband-MIMO Antenna for Ultra-Wideband Applications** 335-340
Lovish Matta, Bhanu Sharma and Manish Sharma
74. **Low Power Bio-Amplifier Using Charge Distribution Technique at CMOS 45nm Technology:A Review** 341-345
Anilsagar Pothana, Tarun Kollati , Sobhit Saxena and Suman Lata Tripathi

5th International Conference on “2023 Devices for Integrated Circuit (DevIC)”

75. **Design of an IoT Based Smart Medicine Box** 346-349
Patan Salman Khan, Manoj Singh Adhikari, Gangadhar Senapathi, Bhawna Chatterjee, Duvyu Vinodh Reddy and Praveen Malik
76. **Study on Effect of Si-SiO₂ and SiGe-HfO₂ to Design 8nm Double Gate MOSFET with Applications** 350-354
Shrabanti Kundu and Jyotsna Kumar Mandal
77. **Design and Analysis of High-Efficiency Eco-friendly Lead-free Perovskite Solar Cell with TiO₂ and C60 Electron Transport Layers** 355-358
Rabin Paul, Shweta Shukla, Trupti Ranjan Lenka, Fazal Talukdar, Nour El Islam Boukortt and Hieu Pham Trung Nguyen
78. **Schottky barrier height modulation of Metal-WS₂ contact by molecular doping technique** 359-363
Arpita Roy, Santanu Sharma and Biplob Mondal
79. **Graphene Nanoribbon based Triple Barrier Double Quantum Well Resonant Tunnelling Diode** 364-367
Madhusudan Mishra, Narayan Sahoo, Trinath Sahu, Nikhil Ranjan Das, Sukanta Kumar Tripathy and Naba Kanta Sahoo
80. **Design of DC-DC Boost Converter Using PFM Switching Technique** 368-371
Maliha Naaz, Kaleem Fatima, B.Rajendra Naik, Shaik Abu Anzar Sayeed, Syed Saquib Ahmed and Mohammed Shahzaib Ashher
81. **Assessing the Impact of Defects on Energy Dissipation of QCA LT Gate using ML Models** 372-376
Manali Dhar, Chiradeep Mukherjee, Ananya Banerjee, Debasmita Manna, Saradindu Panda and Bansibadan Maji
82. **A DC-DC Boost Converter using PWM with 65%efficiency** 377-382
Maliha Naaz, Kaleem Fatima, B.Rajendra Naik, Mohammad Ibrahim, Asfiya Jabeen and Syed Junaid Hussain
83. **Ultra-low-power 4th order quasi-floating gate class- AB flipped source follower filter for biomedical Applications** 383-386
Diksha Thakur and Kulbhushan Sharma
84. **Sensitivity Enhancement of Capacitive MEMS Accelerometer by Design of the Device Geometry** 387-391
Mahua Raha Patra, Kalyan Biswas
85. **Impact of Doping and Temperature on Mobility in Single and Dual Core S/D GAA FinFETs** 392-395
Rupam Goswami, Dwipayana Nath, Prachuryya Das, Priyam Pathak, Deepjyoti Deb and Hirakjyoti Choudhury
86. **IoT Based Smart Work Jacket for Coal Miners** 396-399
Manoj Singh Adhikari, Sabbisetty Phanindra , Balla Chiru Chandana Surya Hasa , Rudra Prasada Rao, Sura Jaya Kumar Reddy and Praveen Malik
87. **Nano porous Structure formation on Multicrystalline Silicon Surface by using Chemical Etching method** 400-403
Sangeeta Barua, Sikha Bandyopadhyay and Sayan Chatterjee

5th International Conference on "2023 Devices for Integrated Circuit (DevIC)"

88. **FPGA Implementation of Area Efficient 16-Bit Vedic Multiplier Using Higher Order Compressors** 404-407
P Sairam, K Manikumar, K Manikumar, B Uday Narayana and K.V.Gowreesrinivas
89. **Statistical Analysis of Integration of renewable DGs in IEEE-9 Bus System using ETAP Simulation** 408-412
Pooja Jain, Ankush Tandon, Divam Pareek and Asheesh Verma
90. **An exhaustive review on recent advances in paper-based microfluidic device for malaria diagnosis** 413-418
Tummalapalli Mounika, Saibaba Vemula, Puppala Lakshmi Usha, Shaik Afroz and Jasti sateesh
91. **Analysis of FLC technique with P&O Algorithm under variable weather condition** 419-424
Firdos Ahmed Eshete, Dip Prakash Samajdar, Anil Kumar
92. **Temperature Sensitive analysis of Junctionless Nanowire Ferroelectric Field Effect Transistor (JNFe- FET) for Enhanced Analog Performance** 425-429
Shalu Garg, Jasdeep Kaur, Anubha Goel, Subhasis Haldar and R.S. Gupta
93. **Comparative Performance between V/F and Rotor Flux-Oriented Controls of Induction Motor Drive** 430-435
Souvik Laha, Jayanta Dhali and Pritam Kumar Gayen
94. **An approach for modeling propagation delay of a subthreshold inverter incorporating DIBL effect** 436-441
Ilika Mitra, Wasim Habib, Silpi Sarkar, Saheli Sarkhel and Soumya Pandit
95. **CNTFET-based design of low power charge pump technique-based voltage multiplier** 442-445
Ricky Rajora, Kulbhushan Sharma, Lipika Gupta and Ashish Sachdeva
96. **Early Prediction of Cataract using Convolutional Neural Network** 446-450
Shuvam Chakraborty and Susovan Jana
97. **Design and Implementation of Hybrid Full Adder Based 16-bit Multiplication Using FPGA** 451-454
K.V.Gowreesrinivas, B.Usha Sri, S.Saideepak, G.Tarun, I.Sathya sagar
98. **A Review of Low-Power Static Random Access Memory (SRAM) Designs** 455-459
Neetu Rathi, Anil Kumar, Neeraj Gupta and Sanjay Kumar Singh
99. **Biosensing attributes of Trench Double Gate Junctionless Field Effect Transistor** 460-464
Palasri Dhar, Soumik Podder, Sunipa Roy and Souman Bej
100. **Performance Evaluation of Buried Gate Oxide based Negative Capacitance FinFETs** 465-469
Vibhuti Chauhan and Dip Prakash Samajdar

5th International Conference on “2023 Devices for Integrated Circuit (DevIC)”

101. **Analytical Model of Dual Cavity Nanowire Tunnel FET-based Dielectric Modulated Biosensor** 470-475
Saheli Sarkhel, Priyanka Saha, Ankit Dixit, Taha Saquib, Sunil Rathore, Rajeewa Kumar Jaisawal, P. N. Kondekar and Navjeet Bagga
102. **Applications of MOSFET-Based High-frequency Signal Processing Memristor** 476-480
Mourina Ghosh, Pulak Mondal and Gouranga Mondal
103. **Sub-threshold swing analysis for NC-TFET in Low-Power Biomedical Applications** 481-485
Sheetal Singh and Subodh Wairya
104. **Noise Analysis in FinFET-based Analog Circuit with Technology Scaling** 486-489
Mallikarjun Patil, Shashank Banchhor, Sunil Rathore, Rajeewa Kumar Jaisawal, Navneet Gandhi, P. N. Kondekar and Navjeet Bagga
105. **Memory Compiler Performance Prediction using Recurrent Neural Network** 490-495
Sabir Hussain, MA Raheem and Afaq Ahmed
106. **FPGA-based Design of a Fault Injector for Binarized Convolutional Neural Network** 496-500
Sowvik Dey, Arijit Patra And Amiya Karmakar
107. **Design and Analysis of 8x8 SRAM Memory Array using 45nm Technology at 100MHz** 501-506
Namgiri Snehith, E Santosh Kumar and Srinivasa Rao Karumuri
108. **Design and Analysis of Dielectrically Modulated Tunnel FET Embedded Nanocavity for breast cancer cells** 507-510
P Harika, Girija Sravani K, Srinivasa Rao K
109. **Design of Low Power, Low Noise with High Output Swing Preamplifier for Cochlear Implants** 511-515
Navin Kumar, Sourav Nath, Koushik Guha, Krishna Baishnab and Srinivasa Rao Karumuri
110. **Analytical Modeling of Asymmetric Junctionless Dual Material Double Gate MOSFET with Underlap for Enhanced Hot Carrier Reliability** 516-521
Arighna basak, Arpan Deyasi and Angsuman Sarkar
111. **Gate-to-Source Leakage Current Computation in Symmetric Double Gate MOSFET incorporating Short Channel Effects** 522-525
Supratim Datta, Arighna basak and Arpan Deyasi
112. **Analysis of Source, Drain and Gate Field Plated AlGaN/GaN Based HEMT for High Breakdown Voltage** 526-530
Soumak Nandi, Mukesh Kumar, Shashank Kumar Dubey and Aminul Islam
113. **Semi-empirical modeling of rectangular triple gate FinFET incorporating the effect of 2D quantum confinement** 531-536
Pratip Chakraborty, Supratim Das, Sabyasachi Sen, Madhumita Das Sarkar and Ria Bose

5th International Conference on “2023 Devices for Integrated Circuit (DevIC)”

114. **Temperature-based Numerical Simulation investigation of the analog performance of AlGaIn/GaN MOS-HEMT** 537-541
Ruby Mann, Shobha Sharma, Sonam Rewari and R.S. Gupta
115. **DFT Modeling of a MoS₂ Monolayer for C₆H₁₂ and C₄H₈O Detection in Lung Cancer** 542-545
Dikcha Chhetri, Prasanna karki, Sumiran Pokhrel, Pronita Chettri, Bibek Chettri, Sanat Das and Bikash Sharma
116. **Ensemble Learning strategy in modeling of future generation nanoscale devices using Machine Learning** 546-550
Rachita Ghoshhajra, Kalyan Biswas, Mahamuda Sultana and Angsuman Sarkar

Novel 32nm CMOS Ternary 3's Complement Generator

Sudeshna Dutta
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
duttasudeshna665@gmail.com

Snigdha Dutta
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
sduttapr1007@gmail.com

Osman Hossain Siddique
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
osmansiddique97@gmail.com

Rimpa Dey
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
rimpadey2018@gmail.com

Aloke Saha
Department of ECE
Dr. B. C. Roy Engineering College
Durgapur, India
saha81@gmail.com

Abstract— Present study unfolds a new optimized scalable circuit topology to generate the 3's complement of a base-3 input and the corresponding 2-step design strategy with respect to an illustrative 4-trit 3's complement generator is elaborated. A novel idea at step-1 generates the 2's complement of a ternary-input. Next, in step-2 the ternary "1" is added with the 2's complement result from step-1 in order to generate the 3's complement output. The clever hardware optimization strategy applying possible fixed-input to the circuit (wherever applicable) is adopted here for the purpose. The complete 4-trit 3's complement generator is designed on 32nm standard CMOS technology using BSIM4 model parameters with 0.9V supply-rail at 27°C temperature using S-Edit of Tanner EDA. The extensive T-Spice transient simulations with all possible test patterns validate the circuit operation. As per evaluation the proposed circuit produces output with 83.37ps propagation delay, 175.65μW average-power and 14.64×10⁻¹⁵J PDP when operated with 100MHz ternary input.

Keywords—hardware optimization, ternary inverter, ternary k-map, ternary number system, t-spice simulation, 3's complement method

I. INTRODUCTION

Typically the complement method is adopted to represent the negative number in digital arithmetic and hence, to perform subtraction operations without dedicated subtractor hardware [1]. Considering recent related activities presented in [2-5] the complement function is also becoming preferable choice in the field of Machine-Learning (ML), Optical-Arithmetic Logic Unit (Optical-ALU), Image Processing, Data-security and so on. Binary (base-2) is the globally accepted number system for digital computation and hence, the corresponding 2's complement method is regular for aforementioned purpose. The stable ON-OFF feature of practical solid-state device can directly be mapped onto binary "1" and "0" respectively [6-9]. However, increasing device density and associated interconnect complexity for binary based VLSI chip is a matter of great concern [10] mainly due to degrading circuit reliability and performance because of localised heat (hotspot) generation, Fan-in/out issue, fabrication complexity etc.

As per study carried out in [11-12] the Multi Valued Ternary (base-3) Logic can be a potential alternative to conventional binary (base-2) counterpart in order to reduce the interconnect complexity and the related hazards by utilizing less number of circuit elements for equivalent data processing. Use of three symbols namely, "0", "1" and "2" in

ternary-system instead of two ("0" and "1" as used in binary-system) is responsible to carry more information as compared to its binary counterpart with same number of digits and eventually reduces the fan-in/out loading issues in an Integrated Circuit (IC) [7-8]. The 3's complement generator is an integral part to carry arithmetic operation in ternary domain [13]. However, with the best of our knowledge a very incremental focus has been observed in open literature in related work.

This work explores a new optimized circuit strategy to generate the 3's complement of a ternary input. The idea is illustrated and presented with respect to a 4-trit ternary input. The conventional normal process E-MOS transistor is applied to optimize the proposed 3's complement generator on 32nm standard CMOS technology with 0.9V supply rail at 27°C temperature. Ternary symbols "0", "1" and "2" are denoted with 0V, 0.45V and 0.9V respectively. The extensive T-Spice simulation with all possible test pattern is carried out in order to validate the design. The Piece Wise Linear (PWL) input source of Tanner EDA is used to generate the custom test patterns for simulations. The evaluated speed-power response of the circuit is recorded.

The rest of the paper is organized as follows: The theoretical aspect of proposed 3's complement generator is explored in section-II. The MOS-level design and corresponding simulation outcome is presented in section-III. Finally, the paper is concluded in section-IV.

II. PROPOSED 3'S COMPLEMENT GENERATOR

This section explains the two-step strategy to construct the proposed 3's complement generator with normal process E-MOS transistor. The signal flow structure with respect to 4-trit ternary input $\{X_3 X_2 X_1 X_0\}$ is presented in Fig.1. The corresponding 2's complement and 3's complement result is represented with $\{Y_3 Y_2 Y_1 Y_0\}$ and $\{Z_3 Z_2 Z_1 Z_0\}$ respectively (Fig.1). Here, X_3 , Y_3 , Z_3 and X_0 , Y_0 , Z_0 represents the MST (Most Significant Trit) and LST (Least Significant Trit) of "X", "Y" and "Z" respectively.

Before proceeding with circuit operation it should be noted that the ternary system offers 3-types of inverter, namely STI (Standard Ternary Inverter), PTI (Positive Ternary Inverter) and NTI (Negative Ternary Inverter). All three Ternary Inverter (TI) along with Ternary Middle Value Decoder (T-MVD) [14] are the integral part of proposed strategy. The corresponding I/O relation for all three Ternary