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# Novel 32nm CMOS Ternary 3's Complement Generator

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***Abstract*— Present study unfolds a new optimized scalable circuit topology to generate the 3's complement of a base-3 input and the corresponding 2-step design strategy with respect to an illustrative 4-trit 3's complement generator is elaborated. A novel idea at step-1 generates the 2's complement of a ternary-input. Next, in step-2 the ternary "1" is added with the 2's complement result from step-1 in order to generate the 3's complement output. The clever hardware optimization strategy applying possible fixed-input to the circuit (wherever applicable) is adopted here for the purpose. The complete 4-trit 3's complement generator is designed on 32nm standard CMOS technology using BSIM4 model parameters with 0.9V supply-rail at 27°C temperature using S-Edit of Tanner EDA. The extensive T-Spice transient simulations with all possible test patterns validate the circuit operation. As per evaluation the proposed circuit produces output with 83.37ps propagation delay, 175.65µW average-power and $14.64\times10^{-15}$J PDP when operated with 100MHz ternary input.**

***Keywords—hardware optimization, ternary inverter, ternary k-map, ternary number system, t-spice simulation, 3's complement method***

## I. INTRODUCTION

Typically the complement method is adopted to represent the negative number in digital arithmetic and hence, to perform subtraction operations without dedicated subtractor hardware [1]. Considering recent related activities presented in [2-5] the complement function is also becoming preferable choice in the field of Machine-Learning (ML), Optical-Arithmetic Logic Unit (Optical-ALU), Image Processing, Data-security and so on. Binary (base-2) is the globally accepted number system for digital computation and hence, the corresponding 2's complement method is regular for aforementioned purpose. The stable ON-OFF feature of practical solid-state device can directly be mapped onto binary "1" and "0" respectively [6-9]. However, increasing device density and associated interconnect complexity for binary based VLSI chip is a matter of great concern [10] mainly due to degrading circuit reliability and performance because of localised heat (hotspot) generation, Fan-in/out issue, fabrication complexity etc.

As per study carried out in [11-12] the Multi Valued Ternary (base-3) Logic can be a potential alternative to conventional binary (base-2) counterpart in order to reduce the interconnect complexity and the related hazards by utilizing less number of circuit elements for equivalent data processing. Use of three symbols namely, "0", "1" and "2" in ternary-system instead of two ("0" and "1" as used in binary-system) is responsible to carry more information as compared to its binary counterpart with same number of digits and eventually reduces the fan-in/out loading issues in an Integrated Circuit (IC) [7-8]. The 3's complement generator is an integral part to carry arithmetic operation in ternary domain [13]. However, with the best of our knowledge a very incremental focus has been observed in open literature in related work.

This work explores a new optimized circuit strategy to generate the 3's complement of a ternary input. The idea is illustrated and presented with respect to a 4-trit ternary input. The conventional normal process E-MOS transistor is applied to optimize the proposed 3's complement generator on 32nm standard CMOS technology with 0.9V supply rail at 27°C temperature. Ternary symbols "0", "1" and "2" are denoted with 0V, 0.45V and 0.9V respectively. The extensive T-Spice simulation with all possible test pattern is carried out in order to validate the design. The Piece Wise Linear (PWL) input source of Tanner EDA is used to generate the custom test patterns for simulations. The evaluated speed-power response of the circuit is recorded.

The rest of the paper is organized as follows: The theoretical aspect of proposed 3's complement generator is explored in section-II. The MOS-level design and corresponding simulation outcome is presented in section-III. Finally, the paper is concluded in section-IV.

## II. PROPOSED 3'S COMPLEMENT GENERATOR

This section explains the two-step strategy to construct the proposed 3's complement generator with normal process E-MOS transistor. The signal flow structure with respect to 4-trit ternary input $\{X_3\ X_2\ X_1\ X_0\}$ is presented in Fig.1. The corresponding 2's complement and 3's complement result is represented with $\{Y_3\ Y_2\ Y_1\ Y_0\}$ and $\{Z_3\ Z_2\ Z_1\ Z_0\}$ respectively (Fig.1). Here, $X_3$, $Y_3$, $Z_3$ and $X_0$, $Y_0$, $Z_0$ represents the MST (Most Significant Trit) and LST (Least Significant Trit) of "X", "Y" and "Z" respectively.

Before proceeding with circuit operation it should be noted that the ternary system offers 3-types of inverter, namely STI (Standard Ternary Inverter), PTI (Positive Ternary Inverter) and NTI (Negative Ternary Inverter). All three Ternary Inverter (TI) along with Ternary Middle Value Decoder (T-MVD) [14] are the integral part of proposed strategy. The corresponding I/O relation for all three Ternary

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