

ICCECE

2023

International Conference

On

Computer, Electrical & Communication Engineering

Conference ID # 51049

| SL No | Paper ID | Authors | Paper Title | Country | |
|-------|----------|--|--|--------------|--|
| 1. | 51 | Venkatraman S and Komathi B J | A Review of Multi-Band Reflectarray Antenna Designs with Mutual Coupling Considerations | India | |
| 2. | 258 | Dadoma Sherpa, Dhruva Abhijit Rajwade, Imon Mitra, Dhruva Dhar, Sunita Sharma and Koel Chaudhury | Prediction of Idiopathic Recurrent Spontaneous Miscarriage using Machine Learning | India | |
| 3. | 7 | Md. Shajedul Islam, Sharifur Rahman and Suman Chowdhury | Investigation of Hybrid Power Performance with Solar Module & Wind Turbine in MATLAB | Bangladesh | |
| 4. | 40 | Arka Ghosh, Raja Das, Shreyashi Dey and Gautam Mahapatra | Ensemble Learning And its Application in Spam Detection | India | |
| 5. | 42 | Shibendu Mahata, Mou Das Mahapatra and Ritu Rani De | Optimal Design of $(\alpha + \beta)$ -Order Butterworth Filter and Its Realization Using RL β C α Circuit | India | |
| 6. | 62 | Abdullah Khayyat, Abdulrahman Alharthi, Faisal Almohammadi, Ziyad Almarwani, Tawfeeq Ahmed, Mohammed Alshahat, Youssef Mobarak and Nithiyananthan Kannan | Design And Development Of Cost-Effective Automatic Solar Panel Cleaning System | Saudi Arabia | |
| 7. | 70 | Subhrajit Dey and Soumitra Bhowmick | Comparative Analysis of MIMO Multiuser Signal Detection | India | |
| 8. | 71 | Chandrashekhar Singh, Jagadish Shivamurthy and Asha Garg | Model Based Test Framework for verification of Flight Control Software | India | |

Optimal Design of $(\alpha + \beta)$ -Order Butterworth Filter and Its Realization Using $RL_\beta C_\alpha$ Circuit

Shibendu Mahata

Dept. of Electrical Engineering
Dr. B. C. Roy Engineering College
Durgapur, India
shibendu.mahata@bcrec.ac.in

Ritu Rani De (Maity)

Dept. of Electrical Engineering
Dr. B. C. Roy Engineering College
Durgapur, India
riturani.de@bcrec.ac.in

Abstract—This paper presents the implementation of an optimal fractional-order Butterworth filter (FBF) using the $RL_\beta C_\alpha$, where $0 < \alpha, \beta < 1$, series circuit. Improved Particle Swarm Optimization algorithm is used to determine the coefficients of three s -domain based fractional-order transfer functions that approximate the FBF characteristics, such that the condition of 0 dB gain at DC is satisfied. Stability, roll-off, accuracy, and algorithm convergence for the proposed FBFs are evaluated. The proposed designs achieve significantly lower error as compared to the recent literature. The Bruton transformation, generalized to the fractional domain, is employed to realize inductor-less FBF circuits. Simulations are carried out in OrCAD PSPICE to verify the design feasibility.

Index Terms—fractional Bruton transformation, fractional order Butterworth filter, fractional order circuits, generalized impedance converter, improved particle swarm optimization

I. INTRODUCTION

Fractional calculus is concerned with employing non-integer order differential and integral operators, and may be regarded as a super-set of the classical/traditional calculus [1], [2]. Several definitions of a fractional derivative, such as the Grünwald-Letnikov, Riemann-Liouville, etc., exist in the literature. For example, the Grünwald-Letnikov derivative of order α , where $0 < \alpha < 1$, for a function $f(t)$, is defined by (1)

$$D_t^\alpha f(t) := \lim_{h \rightarrow 0} \frac{1}{h^\alpha} \sum_{j=0}^{\infty} (-1)^j \binom{\alpha}{j} f(t - jh) \quad (1)$$

where $\binom{\alpha}{j} = \frac{\Gamma(\alpha+1)}{\Gamma(j+1)\Gamma(\alpha-j+1)}$ correspond to the binomial coefficients; $\Gamma(\cdot)$ denotes the gamma function. The Laplace transform of (1), subject to zero initial conditions, is given by (2).

$$\int_0^\infty e^{-st} D_t^\alpha f(t) dt = s^\alpha F(s) \quad (2)$$

where s^α is called the fractional Laplacian operator.

The concepts of fractional calculus, when applied to circuit theory, have led to the formulation of generalized definitions for the traditional circuit elements [3]. For example, the impedance of the traditional integer-order capacitor and inductor is $1/(sC)$ and sL , respectively. However, a fractional capacitor of order α and a fractional inductor of order β , where $0 < \alpha, \beta < 1$, are characterized by impedances of

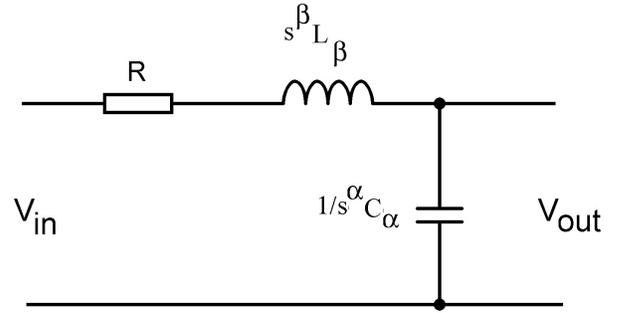


Fig. 1. $RL_\beta C_\alpha$ series circuit acting as a low pass filter.

$1/(s^\alpha C_\alpha)$ and $s^\beta L_\beta$, respectively. The pseudo-capacitance C_α and pseudo-inductance L_β are expressed in units of Farad per second $^{1-\alpha}$ (F/sec $^{1-\alpha}$) and Henry per second $^{1-\beta}$ (H/sec $^{1-\beta}$), respectively [4], [5].

A series RLC circuit can exhibit low pass filter characteristics when the response is considered across the capacitor. Note that there are three free parameters (R , L , and C) for such a circuit. In contrast, an $RL_\beta C_\alpha$ series circuit provides better flexibility in tuning the filter characteristics, since, two additional parameters (α and β) are also now available [6], [7]. An $RL_\beta C_\alpha$ series circuit is shown in Fig. 1. The transfer function for the low pass filter circuit presented in Fig. 1 is given by (3).

$$\frac{V_{out}(s)}{V_{in}(s)} = T(s) = \frac{1}{L_\beta C_\alpha s^{\alpha+\beta} + RC_\alpha s^\alpha + 1} \quad (3)$$

The model represented in (3) exhibits: (i) DC gain of 1 (0 dB), (ii) high frequency gain of 0, and (iii) stopband attenuation of $-20(\alpha + \beta)$ decibel per decade (dB/dec).

A traditional Butterworth filter of order n ($n \in \mathbb{Z}^+$) yields $-20n$ dB/dec attenuation in the stopband [8]. A fractional-order Butterworth filter (FBF) of order $(n + \alpha)$, where $\alpha \in (0, 1)$, can theoretically achieve a roll-off of $-20(n + \alpha)$ dB/dec [9]. Integer-order approximations of FBFs have been carried out using substitution [10] or optimization methods [11]. The design and implementation of the FO transitional Butterworth-Butterworth filter was also recently reported [12]. Various methods were reported to model the analog FBFs