NAME:- SOMYA PRIYADARSHINI
ROLL NO:- 12000119043 , DEPTT:- CSE-I

COMPUTER ORGANIZATION LAB (PCC-CS392)

NAME OF EXPERIMENT:- Implementation of 4 bit Adder Subtractor Composite Unit

APPARATUS USED:-

1. Full Adder
2. Half Adder
3. Full Subtractor
4. Half Subtractor

PIN DIAGRAM:-

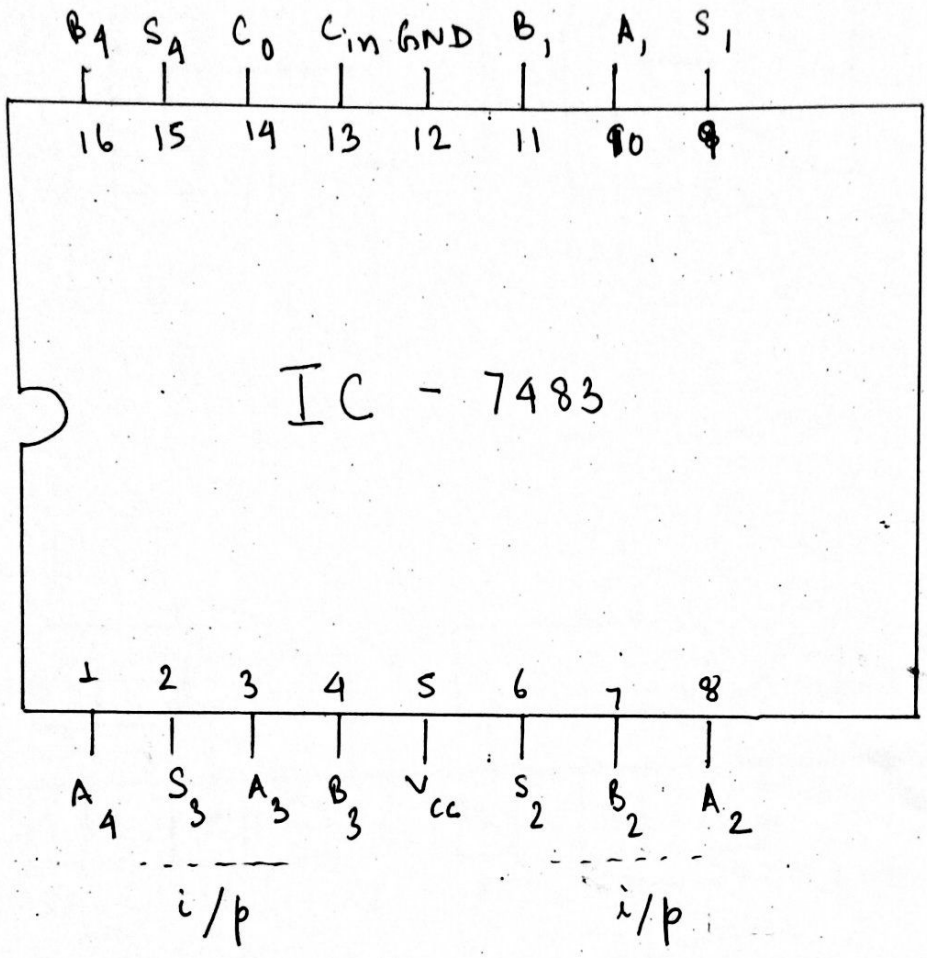


Fig. → Pin Diagram representing of IC-7483

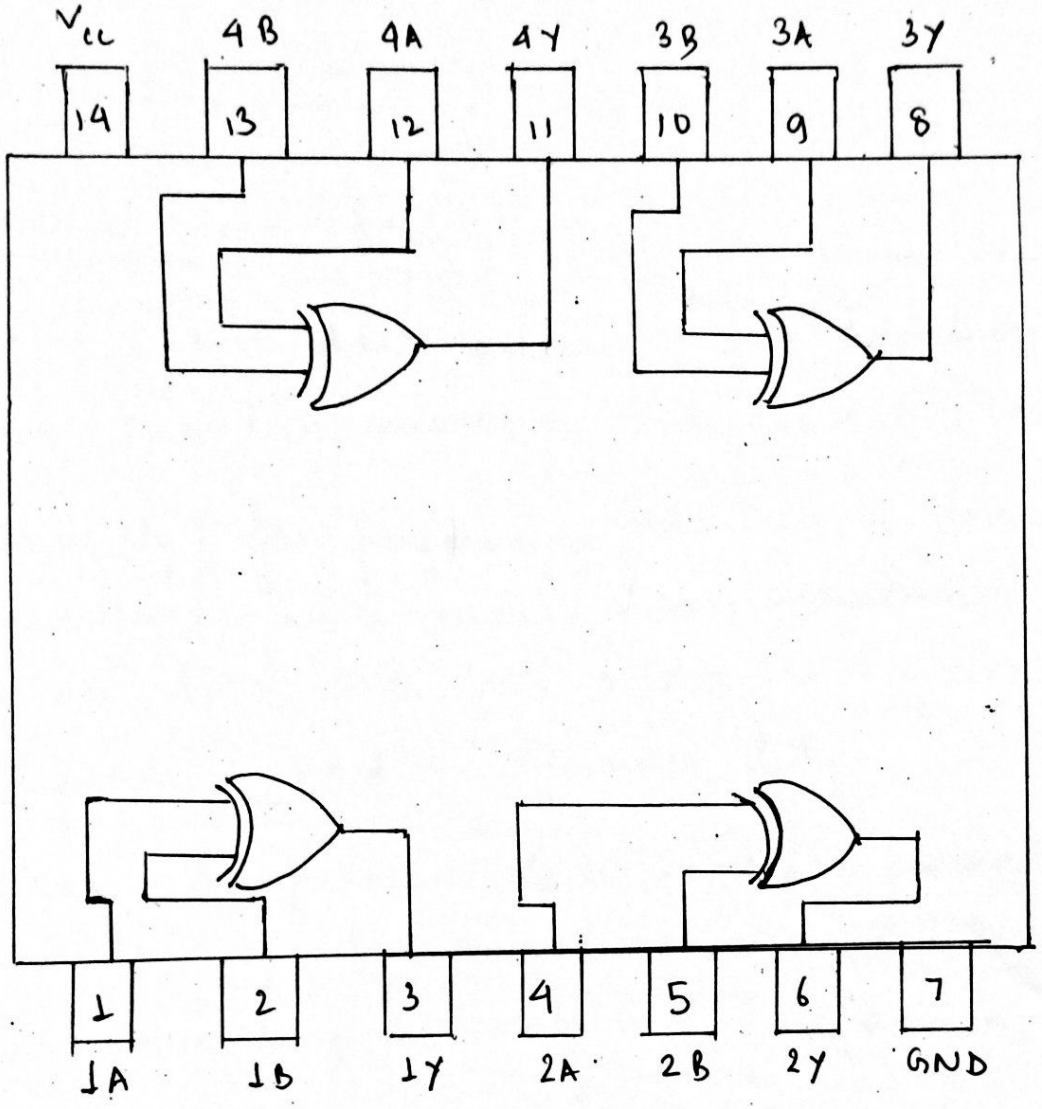
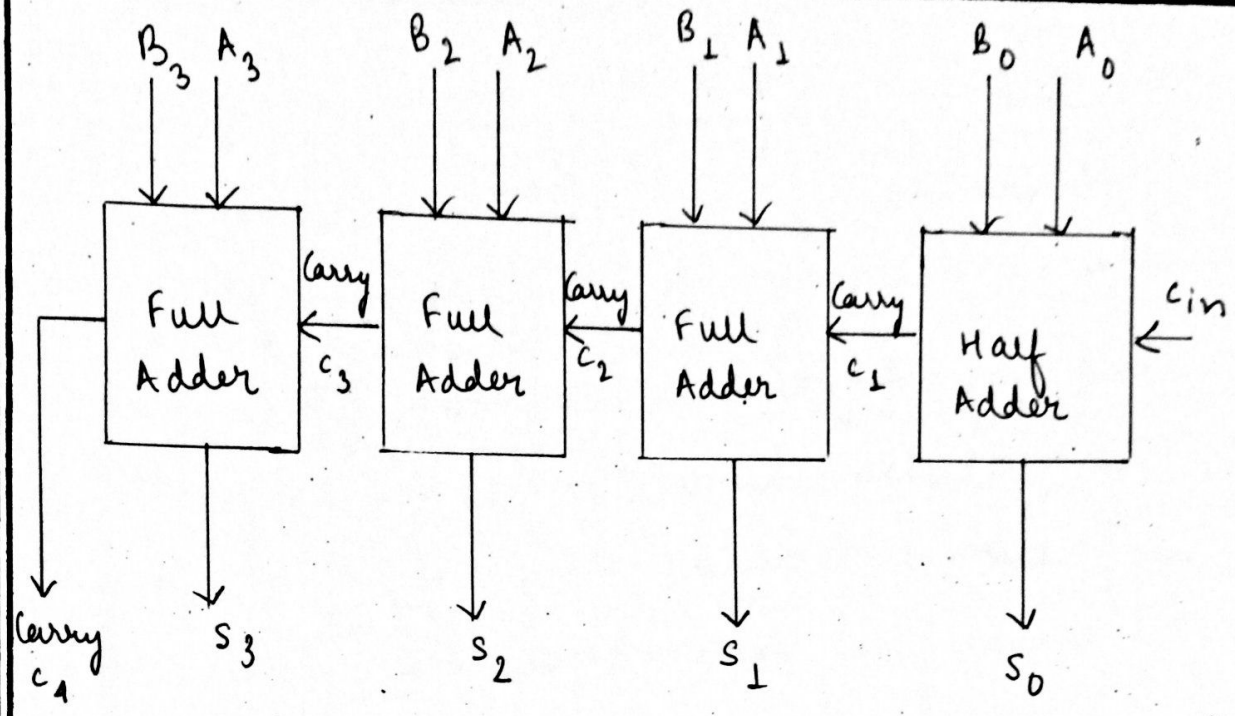


Fig. → Pin Diagram representation of IC-7486

THEORY:-

Parallel Binary Adders:- As, we know that a single full adder performs the addition of two one bit numbers and an input carry similarly, for performing addition of binary numbers with more than one bit, more than one full adder is required depending on the number bits.

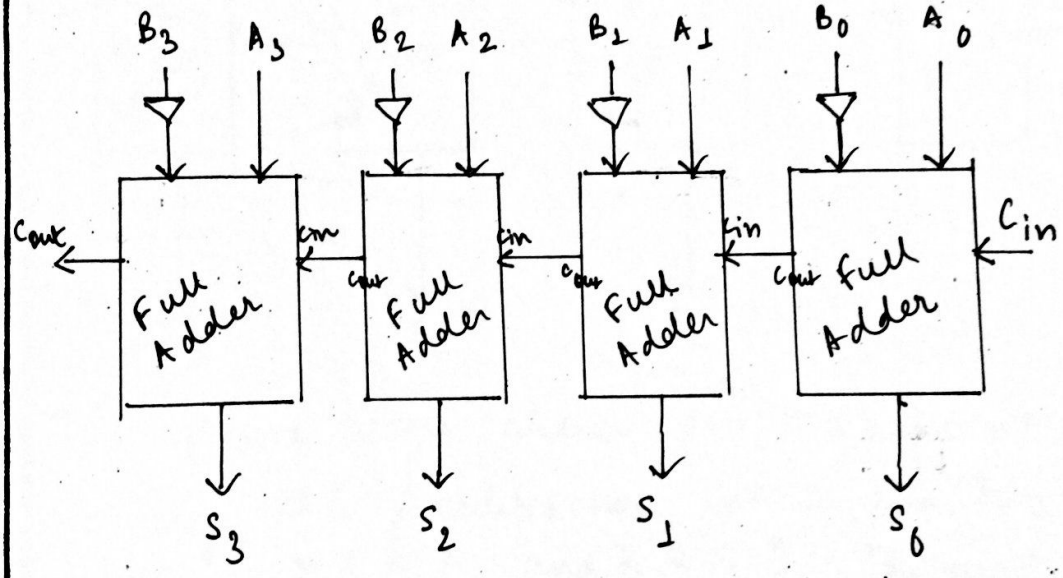
Thus, a parallel adder is used for adding all bits of two numbers simultaneously by connecting a number of full adders in parallel.



The figure above shows a parallel 4 bit binary adder which has three full adder and one half adder. The two binary numbers to be added are $A_3 A_2 A_1 A_0$ and $B_3 B_2 B_1 B_0$ which are applied to corresponding inputs of the adder.

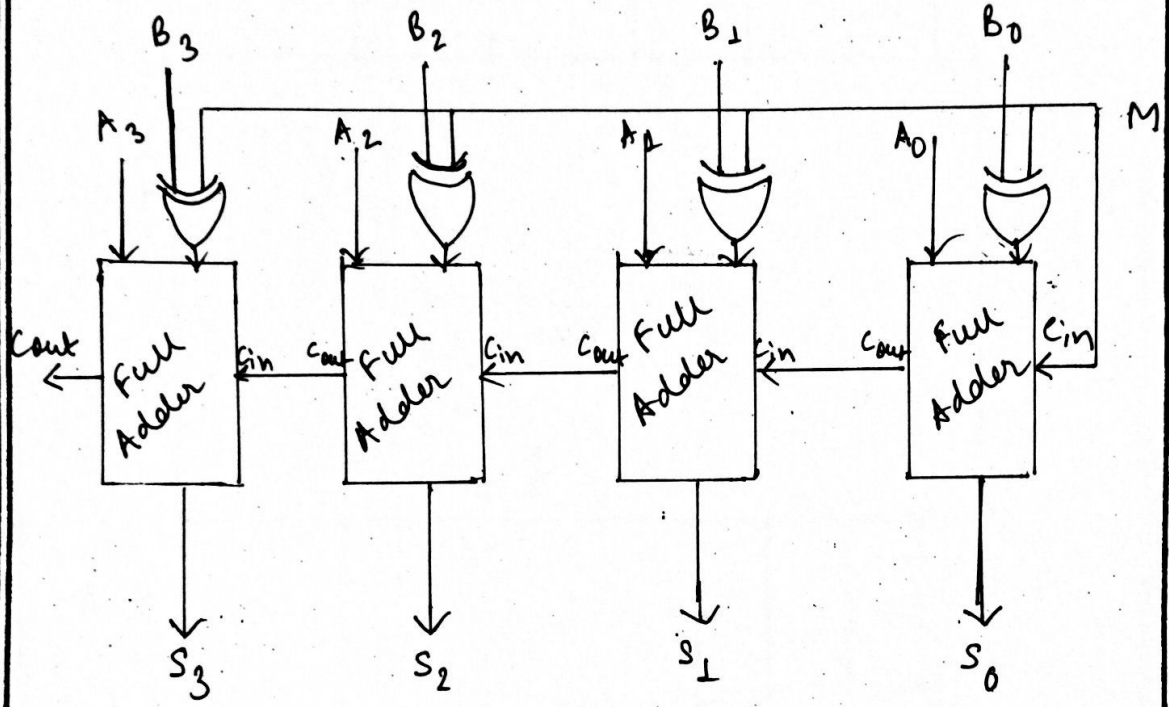
This parallel adder produces their sum as $C_4 S_3 S_2 S_1 S_0$ where C_4 is final carry

Parallel Binary Subtractors :- To perform the subtraction of binary numbers with more than one bit is parallel subtractors are used. This parallel subtractors can be designed in several ways including combination of half and full subtractors, all full adders with subtrahend complement input, etc.



The figure shows a 4 bit parallel binary subtractor formed by connecting 4 full adders. Here $A_3A_2A_1A_0$ is a 4 bit minuend and 4 bit subtrahend $B_3B_2B_1B_0$ is subtracted and output is $D_3D_2D_1D_0$

The operation of both addition and subtraction can be performed by a common binary adder. Such binary circuit can be designed by adding an Ex-OR gate with each full adder.



The figure above shows the 4 bit parallel binary adder/subtractor which has two 4 bit inputs as $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$. The mode input control line M is connected with carry input of the least significant bit of full adder. The control line decides the type of operation.

CIRCUIT DIAGRAM :-

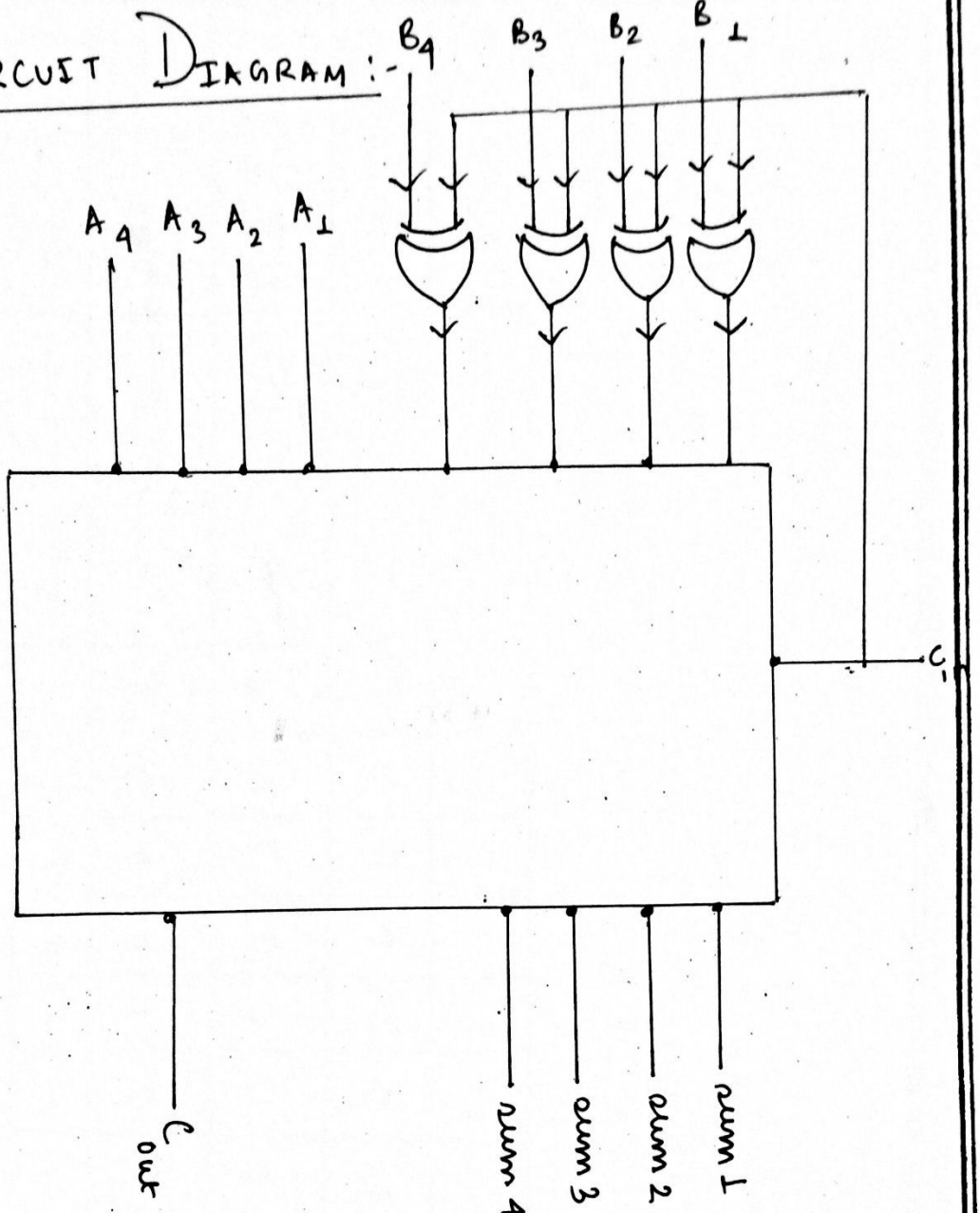


Fig. → Circuit Diagram representing 4 bit Parallel Adder / Subtractor

Truth Table :-

A3	A2	A1	A0	B3	B2	B1	B0	Cin	Cout	S3	S2	S1	S0
1	0	0	0	0	0	1	0	0	0	1	1	0	0
1	0	1	0	1	0	0	1	1	1	0	0	0	1
1	0	0	1	1	0	0	1	0	1	0	0	1	0
...													

CONCLUSION:-

(i) When input control line, M = 1 circuit is subtractor and when its M = 0, circuit becomes adder.

(ii) When M = 0, B Ex-OR of 0 produce B.

(iii) The Ex-OR gate consists of two inputs to which one is connected to the B and other to input M.

(iv) When M = 1, B Ex-OR of 0 produce B complement and also carry input is 1.

Hence the complemented B inputs are added to A and 1 is added through the input carry, nothing but a 2's complement operation. Therefore, subtraction operation is performed.

(v) If $(A > B)$ C_{out} glows as result is true

If $(A < B)$ C_{out} doesnot glows as result is false.