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Speed-Power Efficient Novel CMOS Unary-to-Ternary Encoder

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ABSTRACT

A new full-custom design of Unary-to-Ternary-Encoder (UTE) using standard Enhancement-Type-Metal–Oxide-Semiconductor-Field-Effect-Transistor reporting low-PDP (Power-Delay-Product) and low-area is presented. The inherent pass characteristic of the E-MOS-transistor is exploited here to develop the proposed Ternary-Encoder. Theoretical aspects along with the operation of proposed 9:2 and 27:3 UTE are discussed. The complete UTE is designed and optimized on 32 nm standard CMOS technology at 0.9 V supply-rail and 27°C. Ternary digits "0", "1" and "2" are represented with 0 V, 0.45 V and 0.9 V respectively. The proposed design is validated through extensive T-Spice front-end transient simulations with all possible test patterns. The layout of the proposed design is completed on 32 nm Single-Poly-Double-Metal (SPDM) CMOS–Technology. After DRC and LVS post-layout simulation with extracted parasitic and 1 fF load, is carried out. The valuated performance of the 9:2 UTE is next compared with a recent candidate design to this end, from open literature to benchmark. The Power-Delay-Product (PDP) of proposed UTE is measured by applying ±10% supply variation from nominal on slow, typical and fast MOSFET at −40°C, 27°C and 85°C. Finally, the speed-power characteristic of the proposed 9:2 UTE is explored under different load conditions from 1 to 10 fF.

KEYWORDS

E-MOS pass characteristic; Encoding scheme; PDP (Power delay product); PVT (Process-voltage-temperature) analyses; Transient analyses; Ternary system

1. INTRODUCTION

The base-2 number system is traditionally used to represent information digitally and hence, in related designs from the beginning of the digital era [1,2]. The one-to-one correspondence between binary-digit "1"/"0" with the ON–OFF characteristics of practical solid-state devices makes physical implementation of binary (base-2)digital systems easy and feasible [1–6]. Steady growth and development in sophisticated, smart digital processing along with increased function-density however demanded bringing down interconnect cost and complexity forbase-2-digital design[4–9]. Corresponding fan-in/out hazards [1], localized heat dissipation (hot-spot) [10], delay-mismatch at different circuit locations. degraded overall circuit reliability and robustness. Concurrently, studies on MVL (Multi-Valued Logic) [11–14]revealed "ternary" (base-3) as a feasible alternative to base-2-system to achieve reduced interconnect complexity by utilizing less number of component blocks in the system, reporting thereby improved circuit efficiency, reliability as compared to its binary counterpart. Ternary carries relatively more information for the same number of digits as compared to binary by utilizing 3-logic levels ("0", "1" and "2") instead of 2 (as in binary) to represent digital data [15–20] which results in aforesaid improvement. However, operating on 3-logic levels makes the basic ternary logic cells more complex as compared to binary logic cells and that becomes the challenge to clever design ideas to harvest the benefits.

Encoder [21–24] that produces equivalent coded output based on active unary input is one of the important data path elements for digital processing applications. For n-digit encoding the binary and ternary system selects from 2^n and 3^n input lines respectively. Hence, a ternary system essentially can accommodate $(1.5)^n$ times more input lines for n-digit encoding as compared to binary. The exponential dependence makes ternary encoding preferable especially in sophisticated, high-resolution, smart processing systems due to reduced interconnect and fan-in/out complexity. However, dealing with 3-logic levels is the major bottleneck to improve overall system efficiency. In this work, a clever design strategy for speed-power efficient Unary-to-Ternary-Encoder (UTE) exploiting the inherent advantage of pass characteristics of E-MOS transistor is proposed. The idea is realized by designing and simulating 9:2 and 27:3 UTE circuits using BSIM4 device parameters on 32 nm standard CMOS technology at 27°C temperature and 0.9 V supply-rail with 1 fF load. Trit values "0", "1" and "2" are denoted by 0, 0.45 and 0.9 V respectively. After T-Spice transient validation with all possible test patterns