Efficient 3's Complement Circuit for Ternary-ALU

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***Abstract*—Carrying more information makes the ternary-computation effective with the aim of lowering interconnect hurdle. Hence, ternary computer can be the future alternative to conventional (binary) counterpart. As a consequence the ternary arithmetic has become the prime choice of circuit/system researcher in recent time. Ternary adder/subtractor is the integral part of Ternary Arithmetic Logic Unit (TALU) and 3's complement is used to represent negative ternary number in TALU. Current work unfolds a new two-step low hardware-cost strategy to converts ternary input into its three's complement form. Novel optimization strategy to improve hardware efficiency (i.e. PDP)using conventional Enhancement-type Metal Oxide Semiconductor (E-MOS)-transistor is explored and exploited to design proposed 4-inputthrees complement generator on 32nano-meter standard Complementary-MOS technology with 900mV supply-rail at 27°C temperature using nominal MOS-transistor. Unbalanced trit "0", "1" and "2" are denoted with ground, supply/2 and supply respectively. The circuit transient characteristic is validated through rigorous T-Spice simulations with every possible test patterns and the speed-power result is examined and compared to benchmark. The circuit performance is also evaluated by applying load variation. The 4-trit three's complement circuit is extended next to propose 16-trit 3's complement generator and the impact of Process and Environmental variation on the proposed circuit is studied.**

***Index Terms*—Hardware Optimization, Power-Delay-Product, PVT-Variation, Ternary 3's Complement, Unbalanced Ternary System**

I. Introduction

Higher speed-power efficiency with reduced interconnect complexity is always been at the centre of demand for digital processing [1-2]. Fabrication complexity and the associated hazards owing to large interconnect is the major bottleneck for current binary-based sophisticated digital system implementation [3]. Higher radix or multi-valued system can offer some efficiency by processing relatively more information with less number of logic blocks [2, 4] and attracted researcher from long-back [5-6]. Being closure to natural base-e (≈ 2.78) the multi-valued ternary (base-3) was attracted W. Alexander to investigate ternary-computer in 1964 [7] and also received renewed interest among circuit research community in recent time as evidenced from [8-14]. Complement strategy is trendy to stand for the negative number in digital domain and consequently the 3's complement circuit serves as an essential part for adder/subtractor block in ternary-ALU (Arithmetic Logic Unit) [2, 14-16]. As per recent study [17-19] the complement method is also becoming preferable for Machine andDeep Learning, Data Security, Image Processing etc. Hence, efficient ternary 3's complement circuit is the need of the hour and is investigated in present work.

Most recently in 2022, S. Rani et. al [2] presented a 4-trit ternary adder/subtractor by exploiting T-XOR (Ternary-XOR) based novel 3's complement circuit for low-power, high-speed ternary-ALU. Use of generic T-XOR is the matter of concern and calls for hardware inefficiency and related power-delay hazards. Present study explores a unique two-fold strategy that can optimize the hardware complexity with carry generation/propagation delay of 3's complement circuit. Firstly, the required logic cells are optimized by exploiting input constraint and applying don't care condition. A novel strategy is adopted next to reduce the internal carry generation/propagation delay as well as corresponding hardware cost. Eventually overall speed-power efficiency of the circuit improves in favor of efficient ternary-ALU design. Proposed idea is explained with respect to Four-trit threes complement circuit and is designed using BSIM4 conventional E-MOS transistor on 32nano-meter standard Complementary-MOS technology at 27°C temperature with 900mV supply. Unbalanced trit value "0", "1" and "2" are represented with 0V, supply/2 and supply respectively. The working of proposed circuit is checked through extensive T-Spice transient simulations with custom ternary test inputs. Speed-power response of proposed Four-trit threes complement circuit is then compared with the idea presented in [2] by considering equal operating condition and 0.1GHz test input and 1fF load to benchmark. The power-delay performance of the designed circuit is tabulated in different load (i.e. 1fF to 10fF) value. The circuit is next extended to design 16-trit 3's complement circuit and validated through all possible transient simulations. Finally, robustness with respect to PVT (Process Voltage Temperature) variation is measured and recorded.

The rest part of this paper is organized as follows: Section-II explores the proposed idea to construct 3's complement circuit in detail. Section-III is responsible to present the design, simulation result and benchmarking with most recent competitive work. Section-IV concludes the paper.

II. Proposed 3's Complement Generator: Theoretical Perspective

The block-level data-flow model of proposed ternary three's complement circuit is depicted in Figure-1. The 4-trit ternary input in Figure-1 is represented with "X" {X_3 X_2 X_1 X_0} where X_0 is the LST (Least-Significant-Trit) and X_3 is the MST (Most-Significant-Trit). Corresponding two's

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